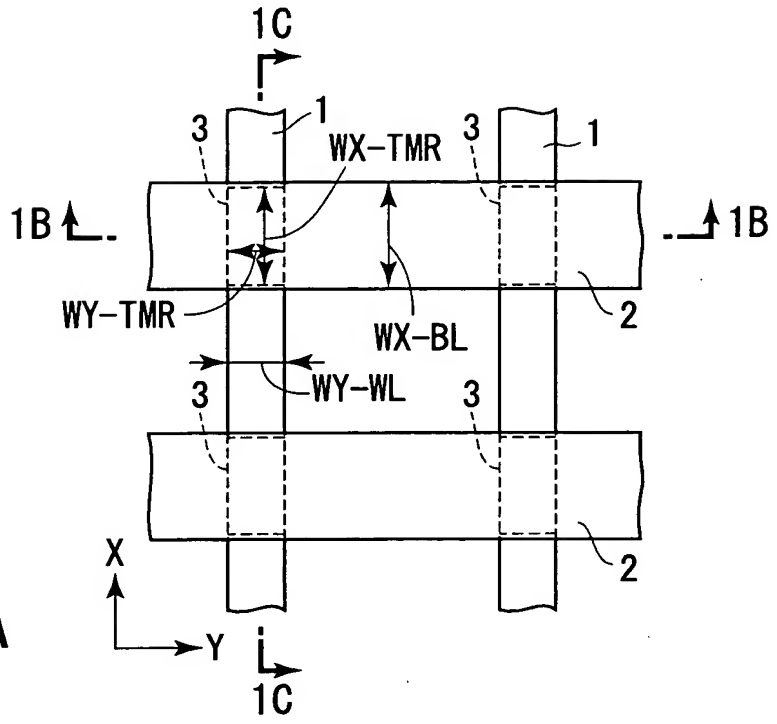

FIG. 1A

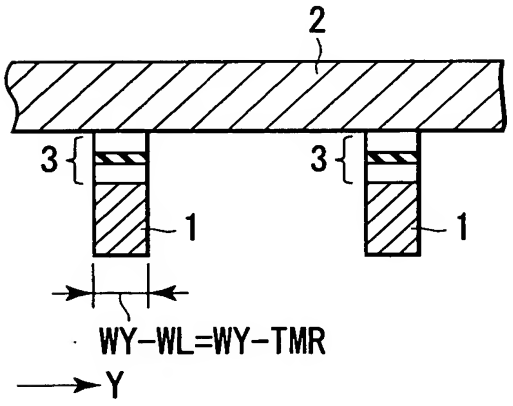

FIG. 1B

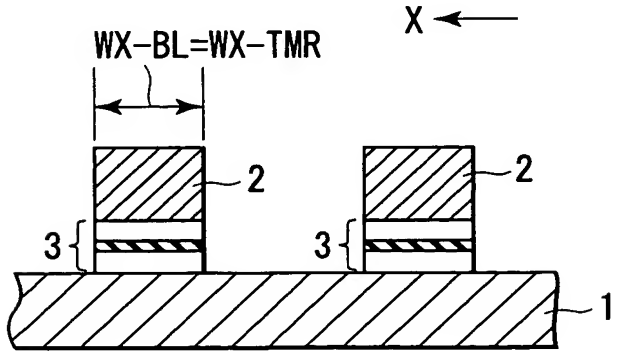

FIG. 1C

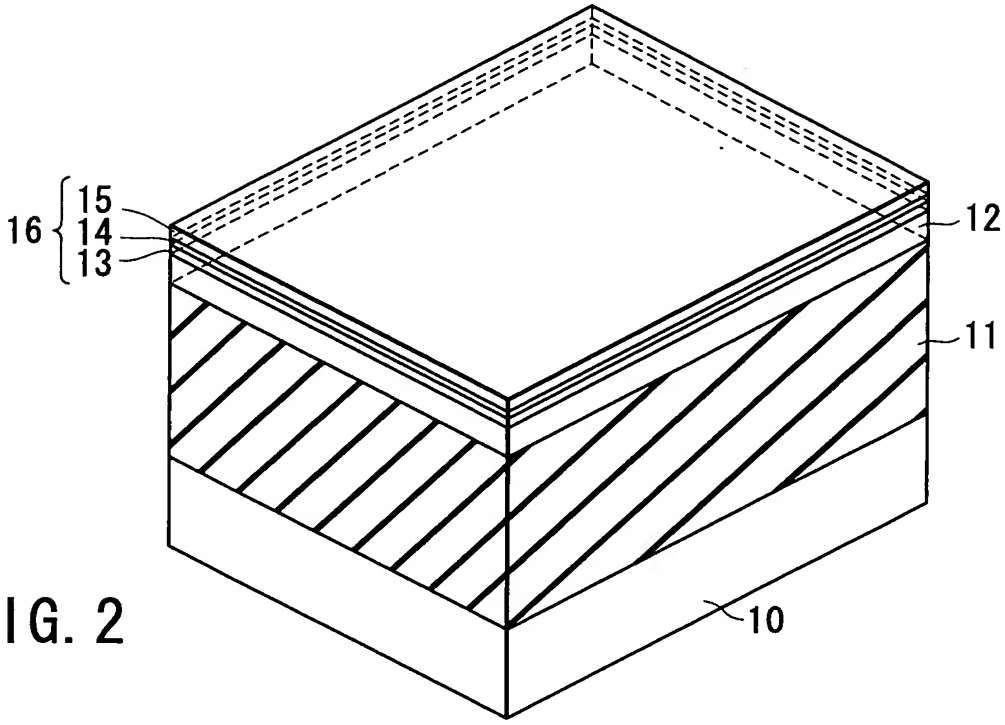

FIG. 2

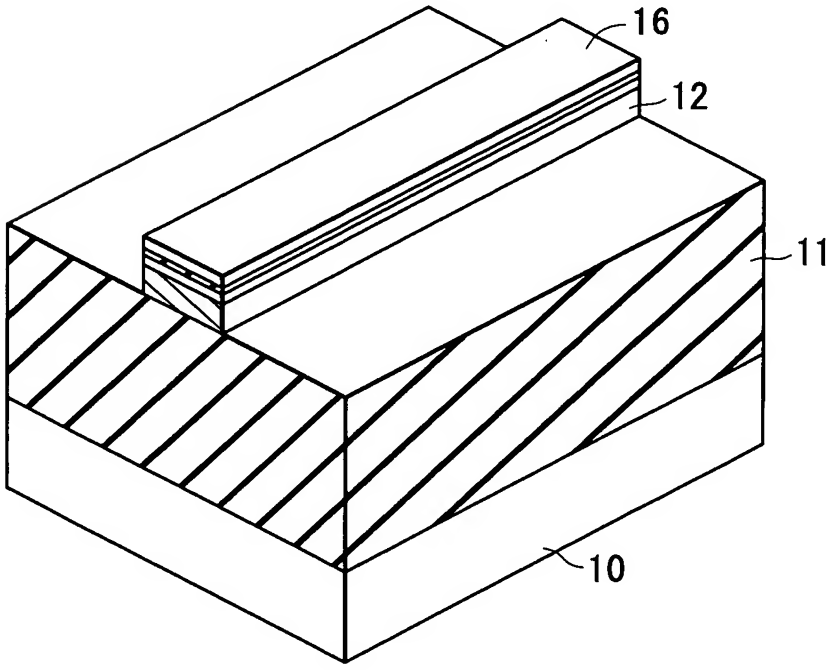

FIG. 3

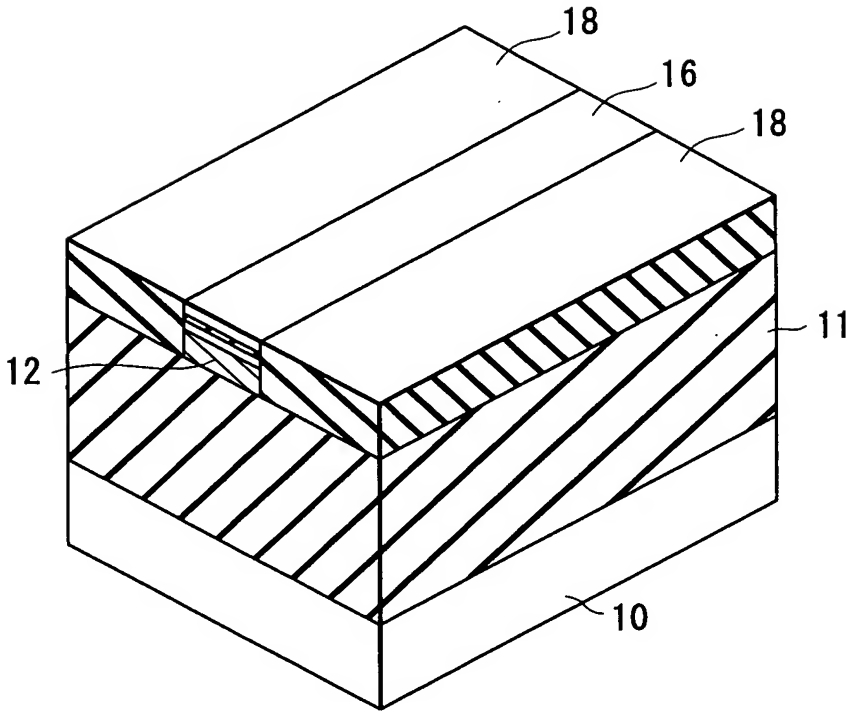

FIG. 4

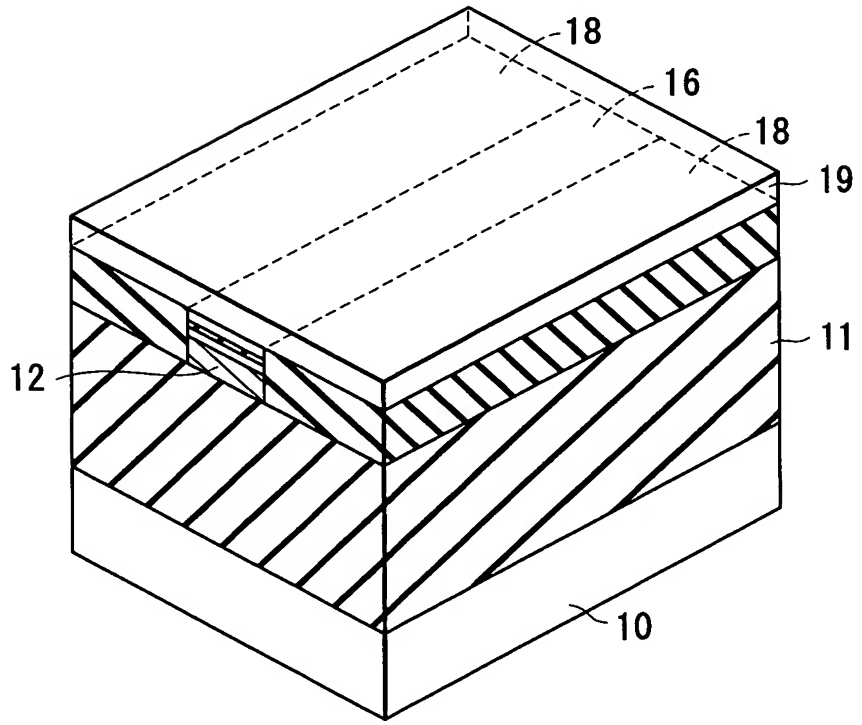

FIG. 5

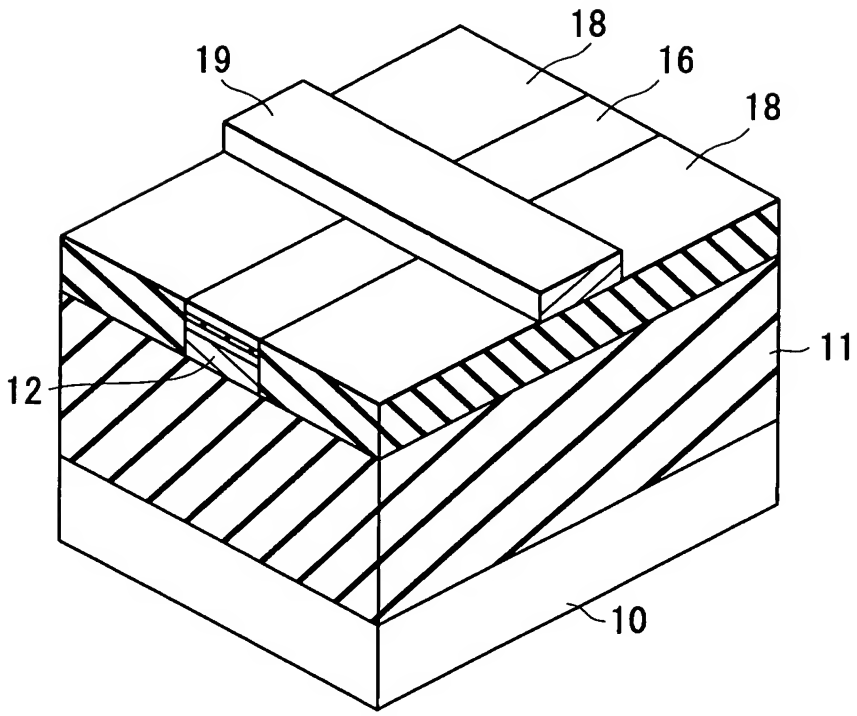

FIG. 6

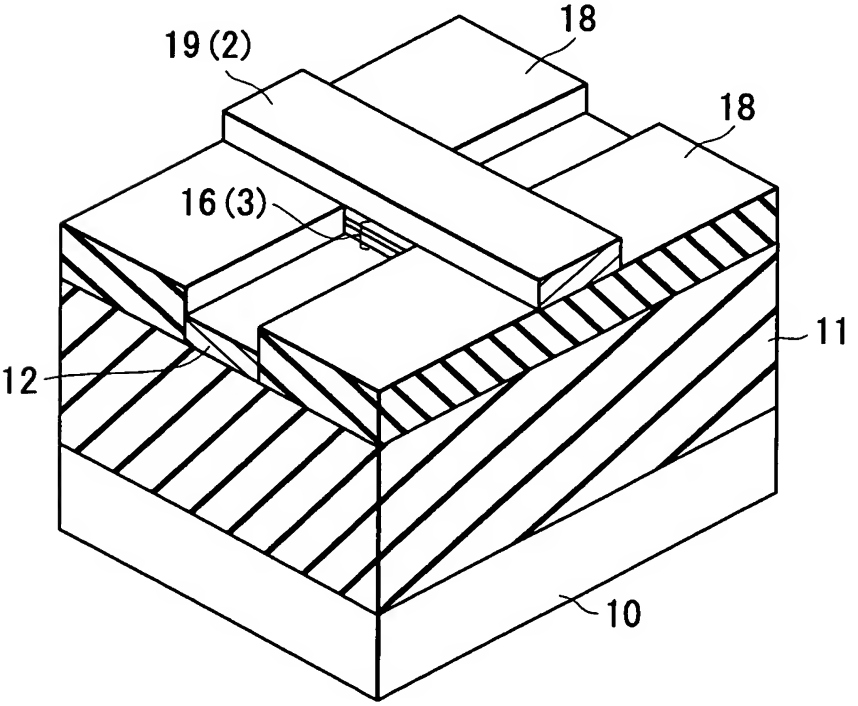

FIG. 7

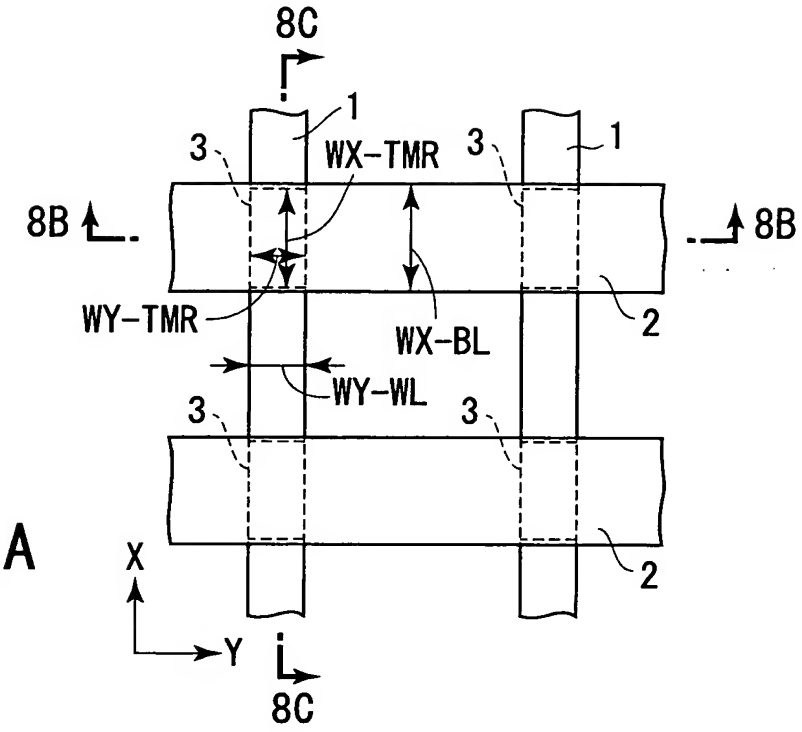

FIG. 8A

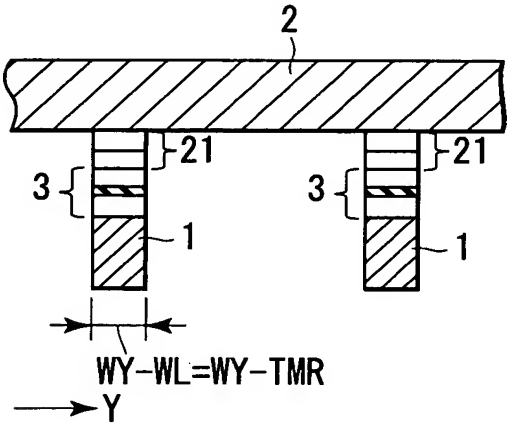

FIG. 8B

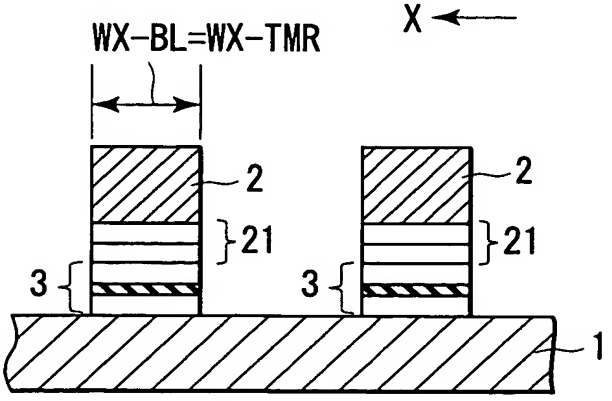

FIG. 8C

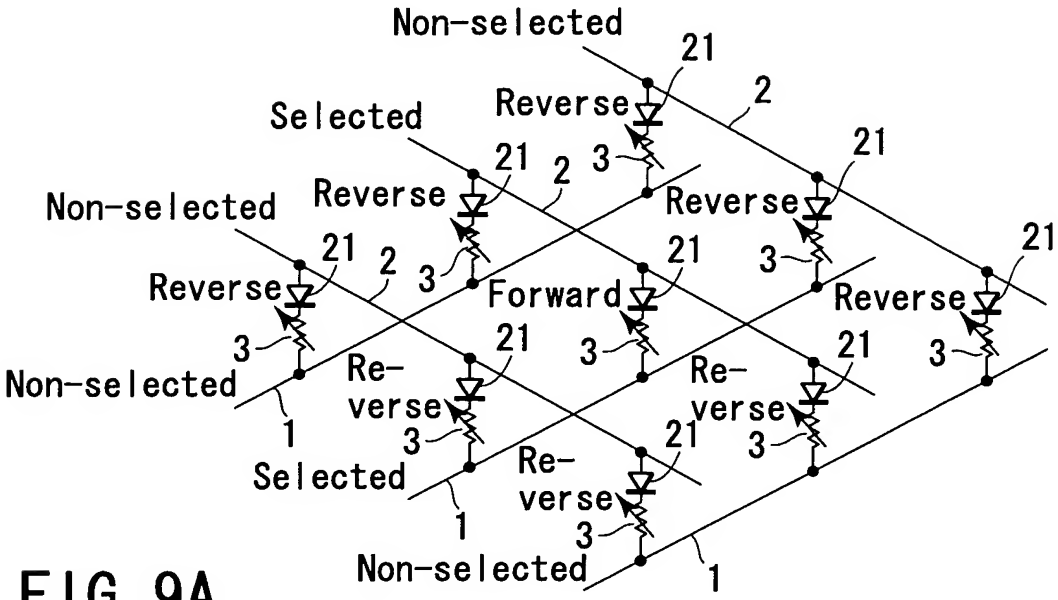

FIG. 9A

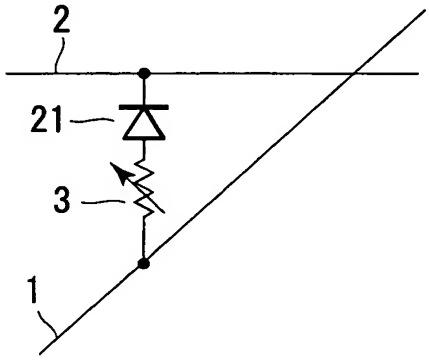

FIG. 9B

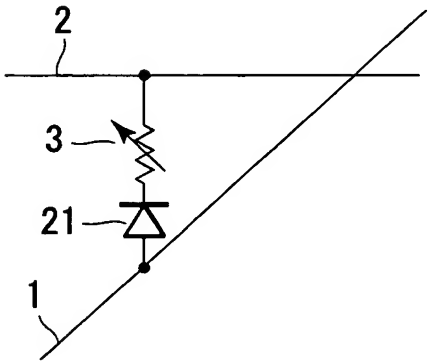

FIG. 9D

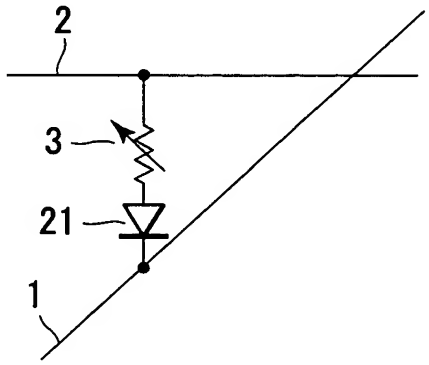

FIG. 9C

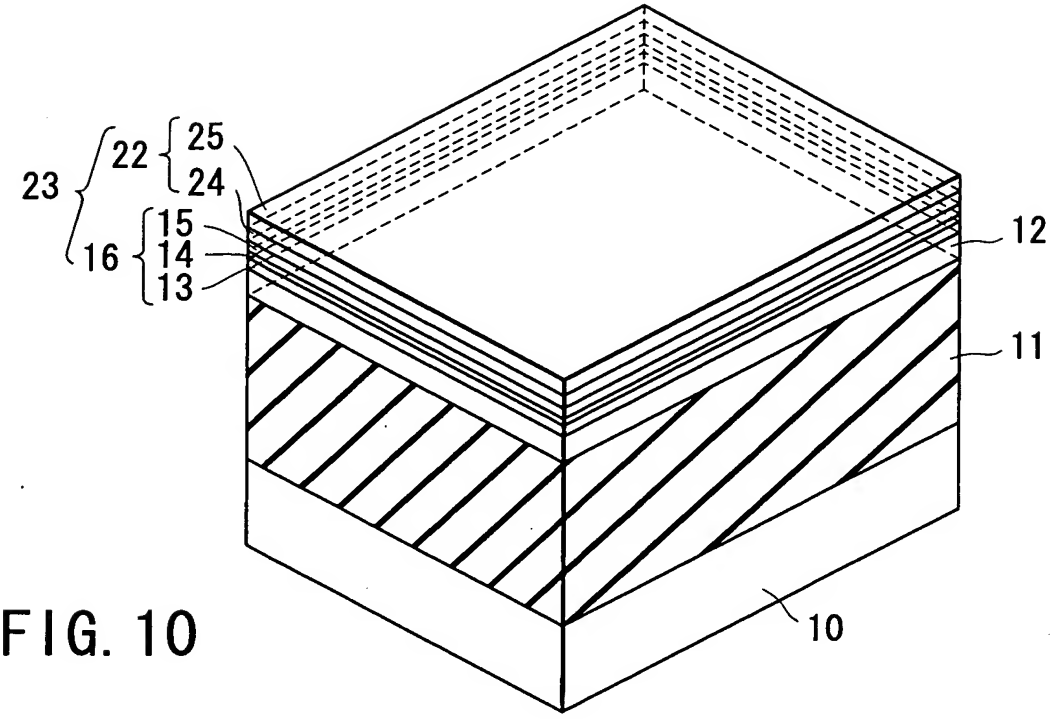

FIG. 10

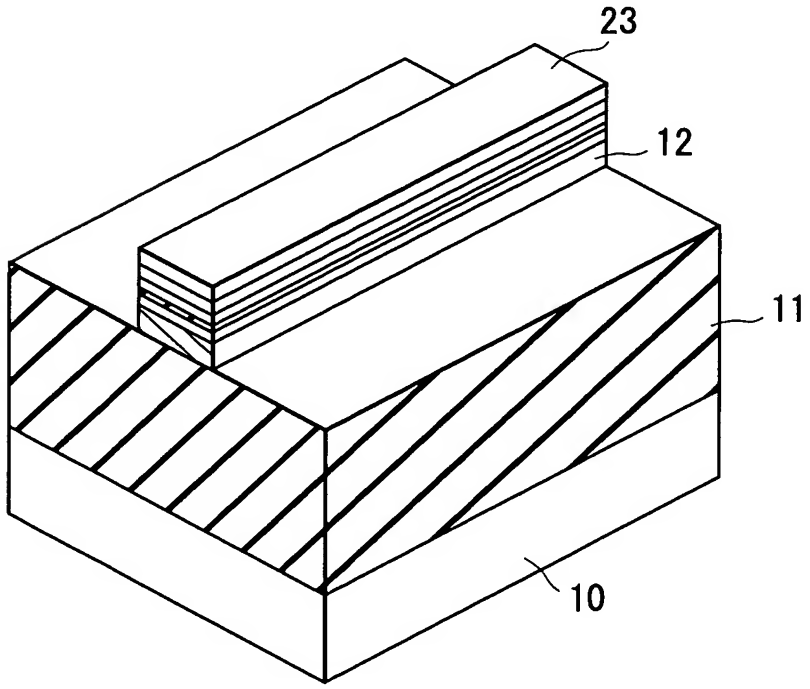

FIG. 11

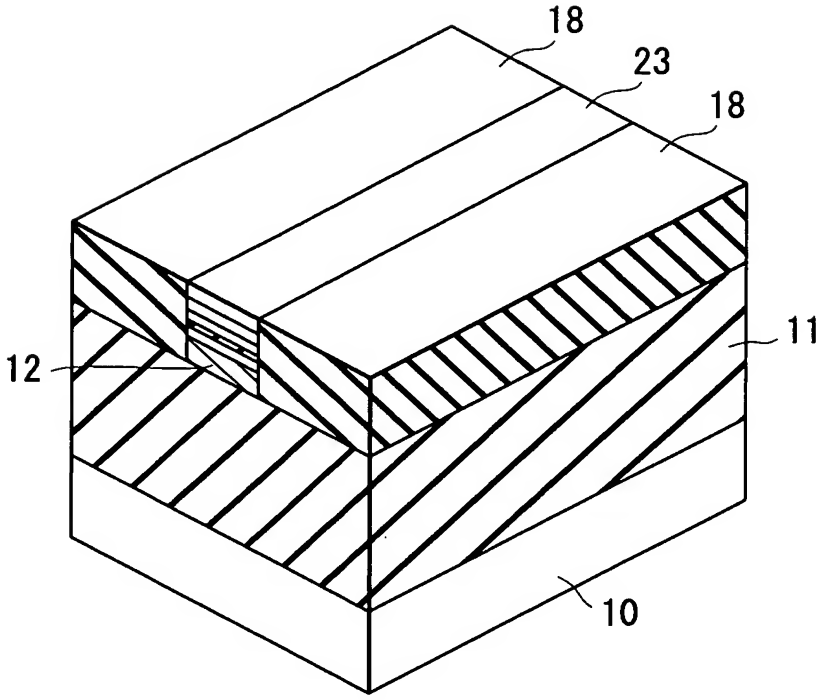

FIG. 12

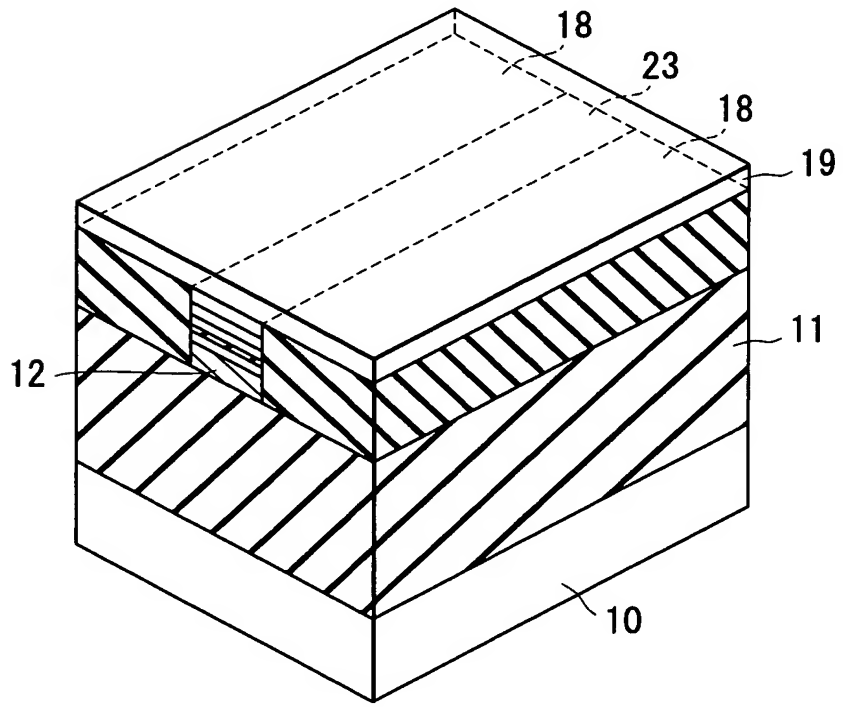

FIG. 13

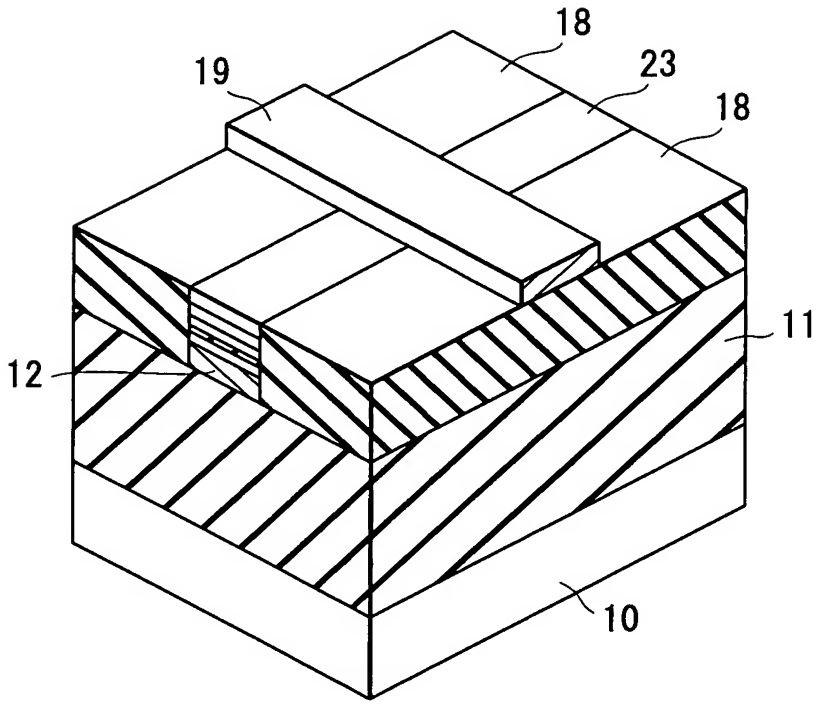

FIG. 14

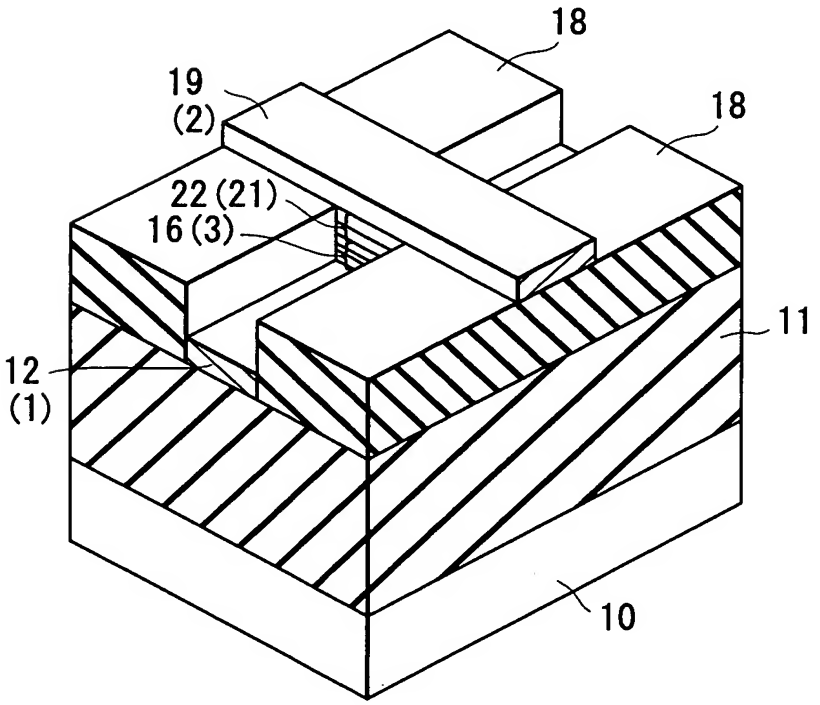

FIG. 15

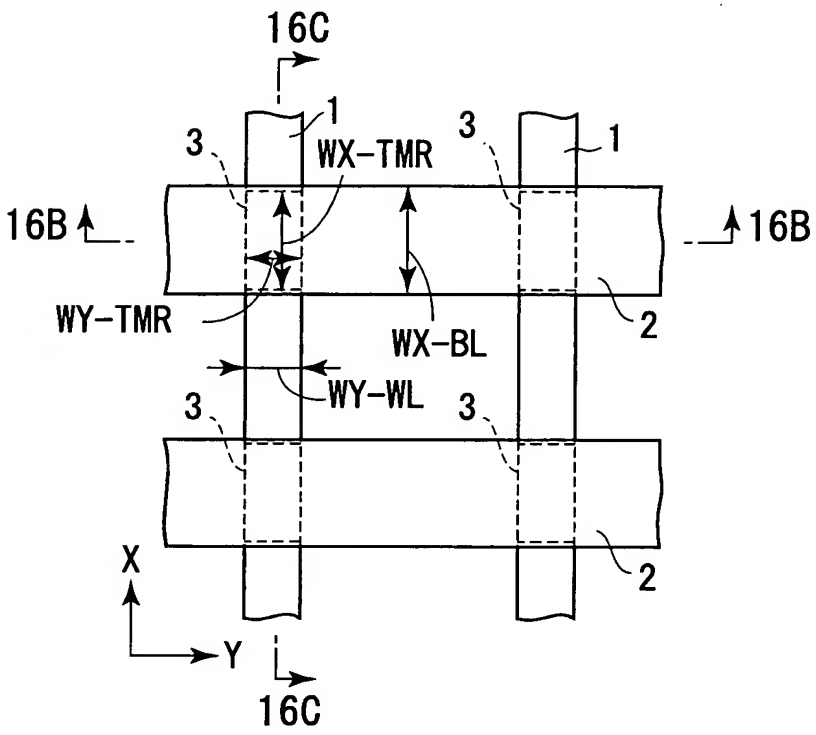

FIG. 16A

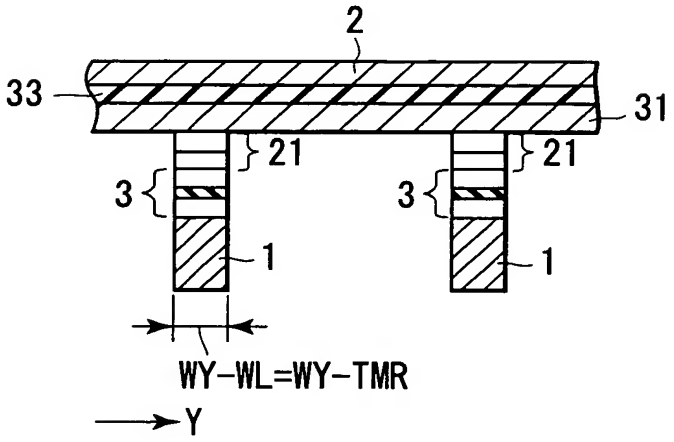

FIG. 16B

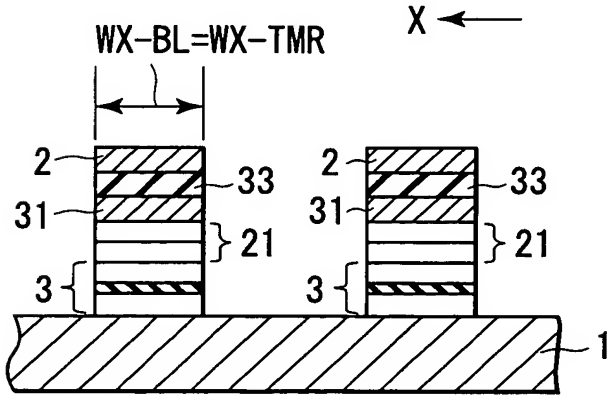

FIG. 16C

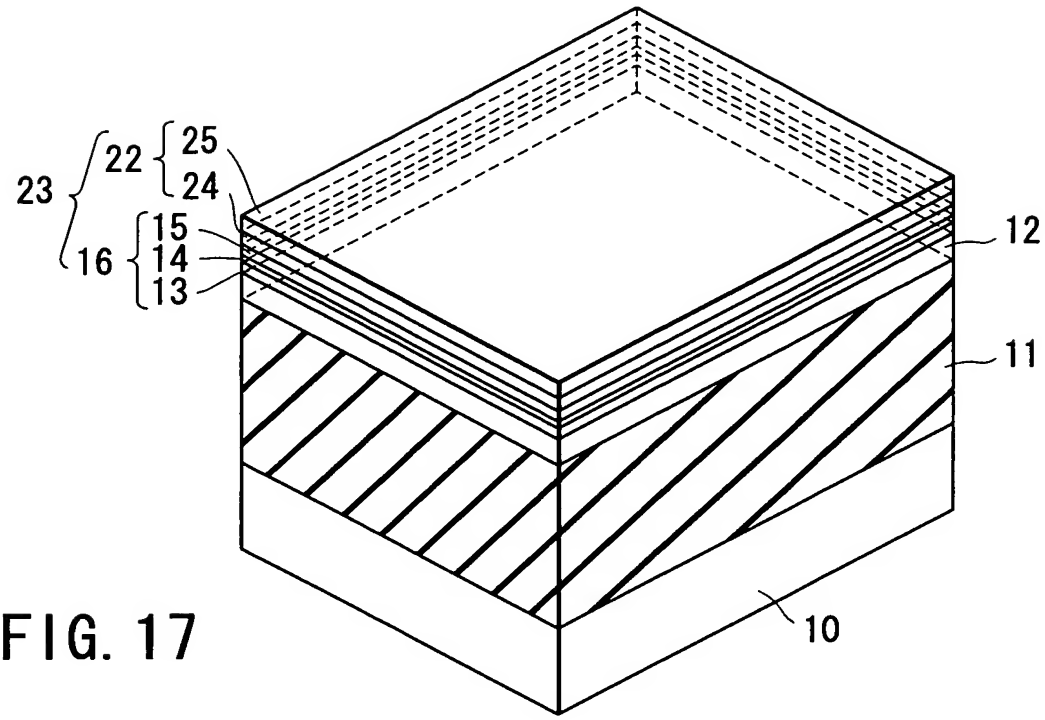

FIG. 17

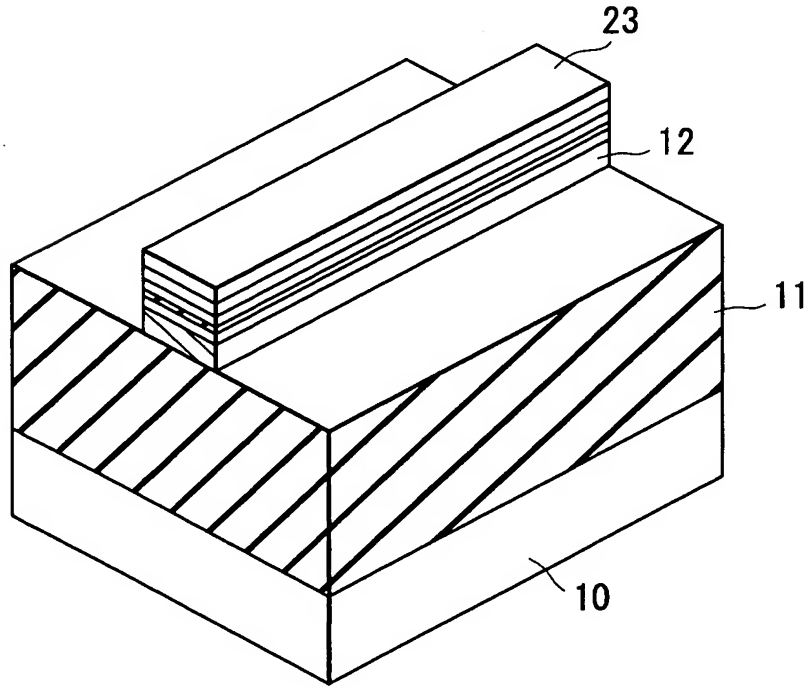

FIG. 18

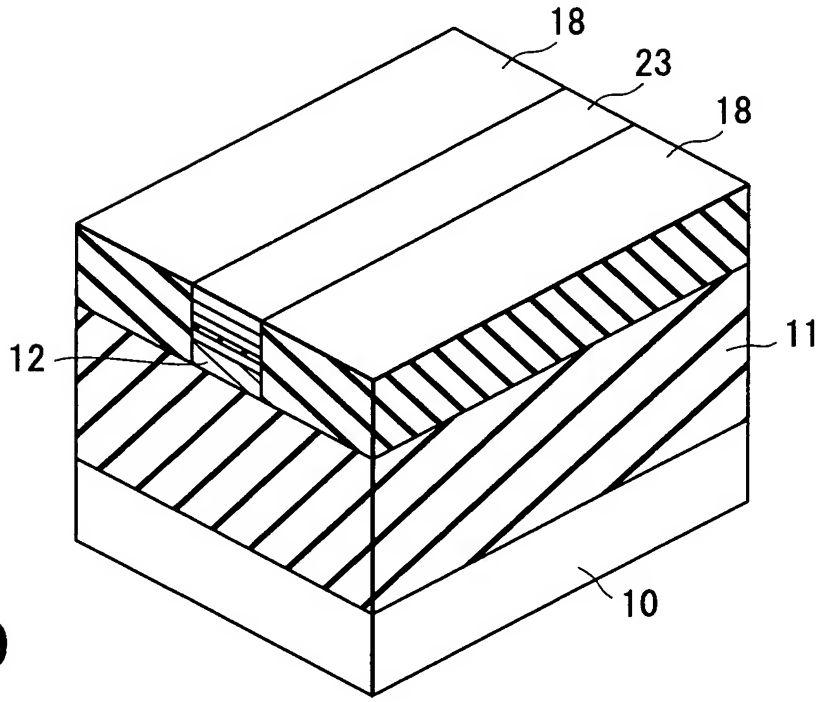

FIG. 19

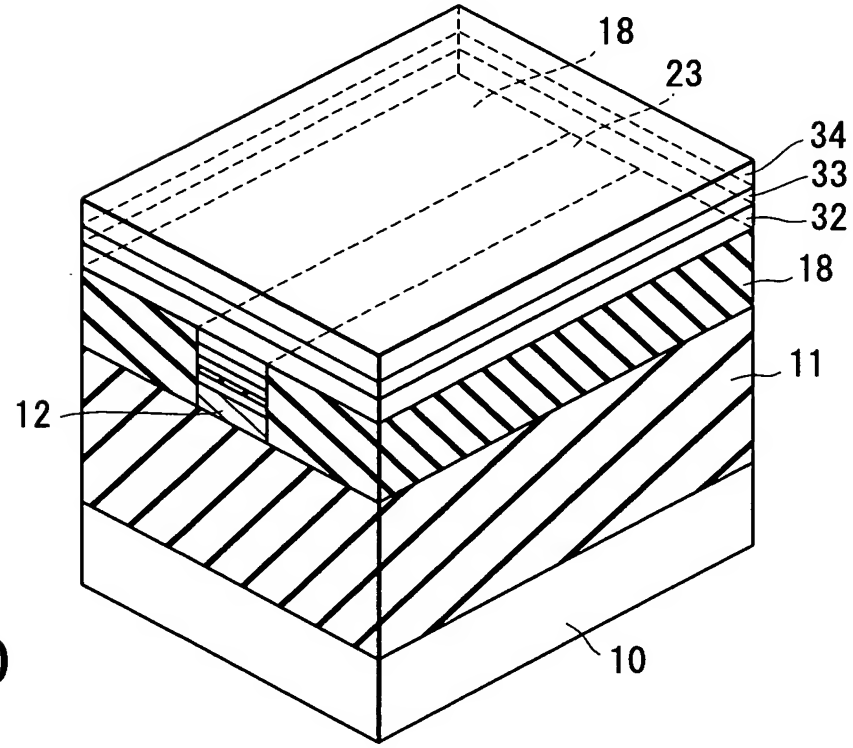

FIG. 20

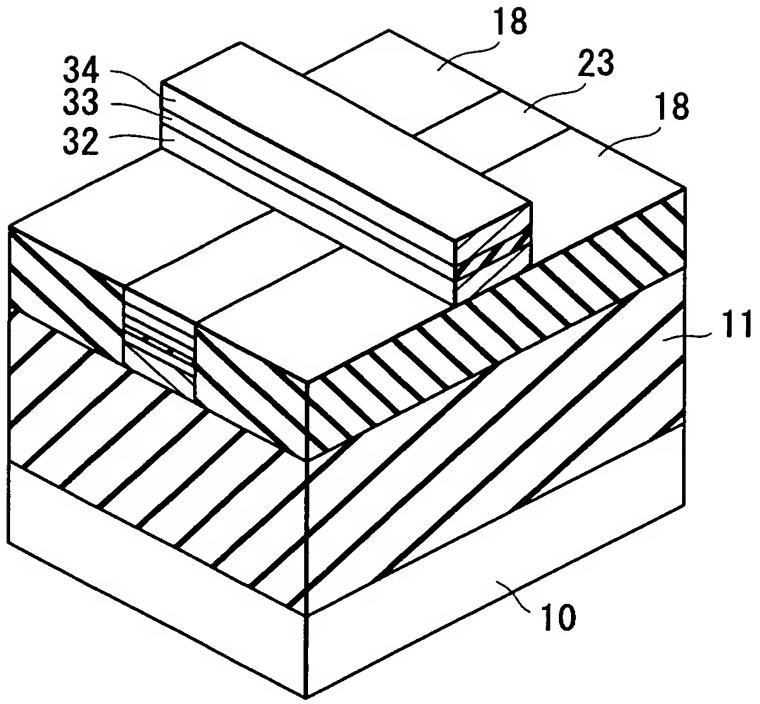

FIG. 21

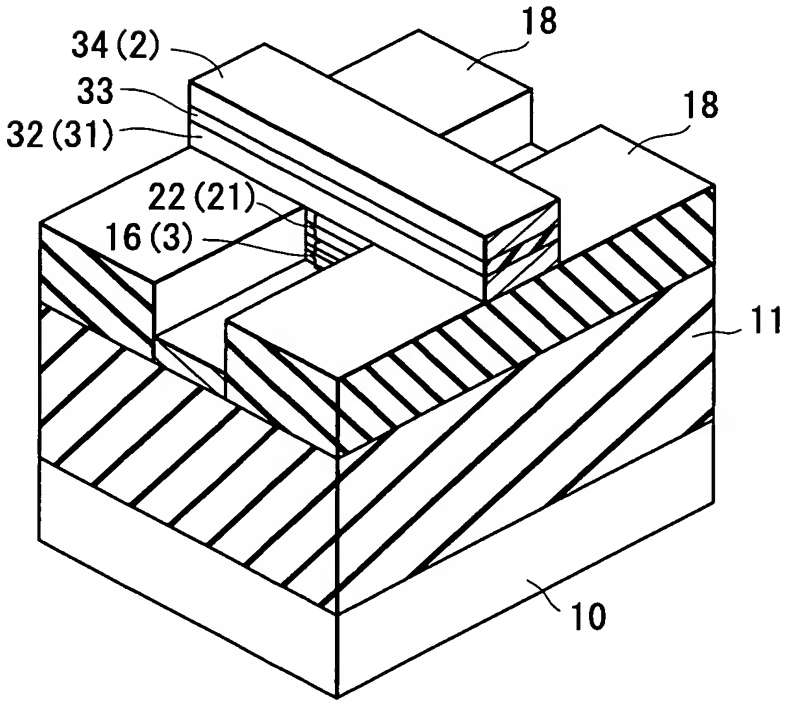

FIG. 22

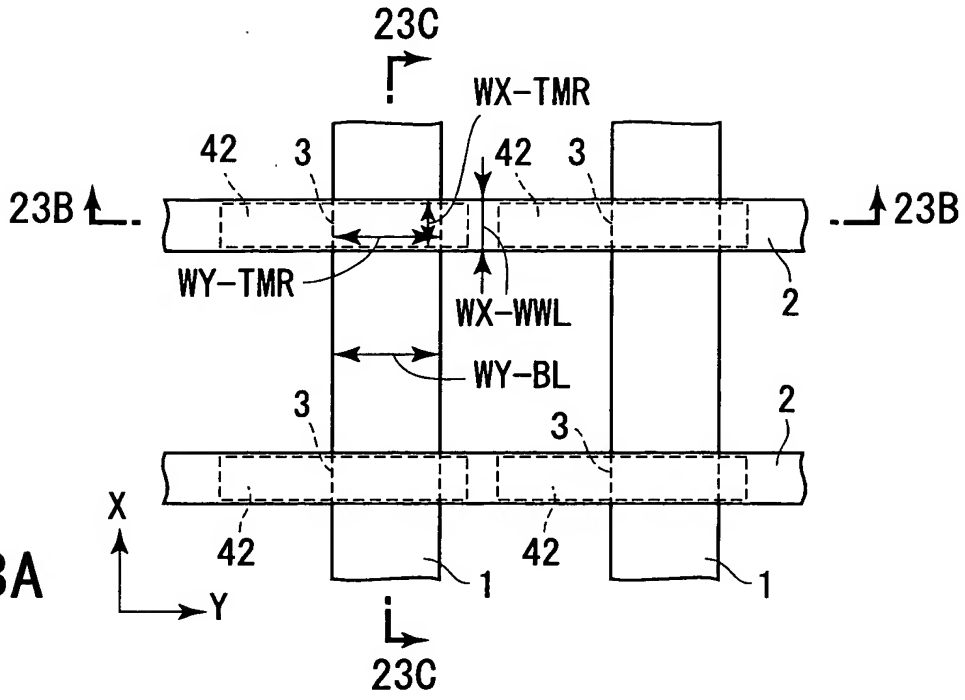

FIG. 23A

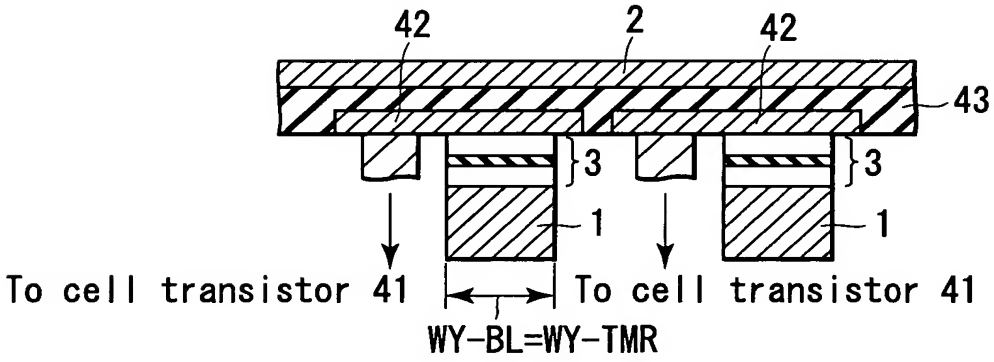

FIG. 23B

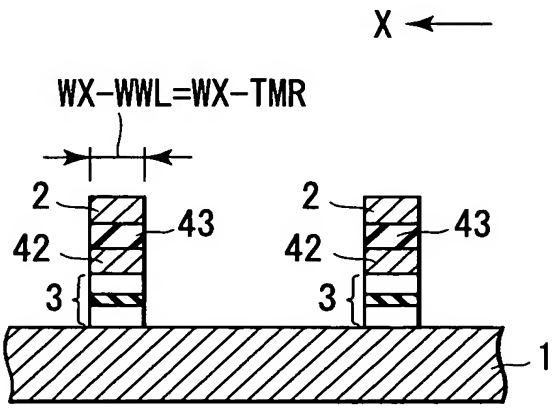

FIG. 23C

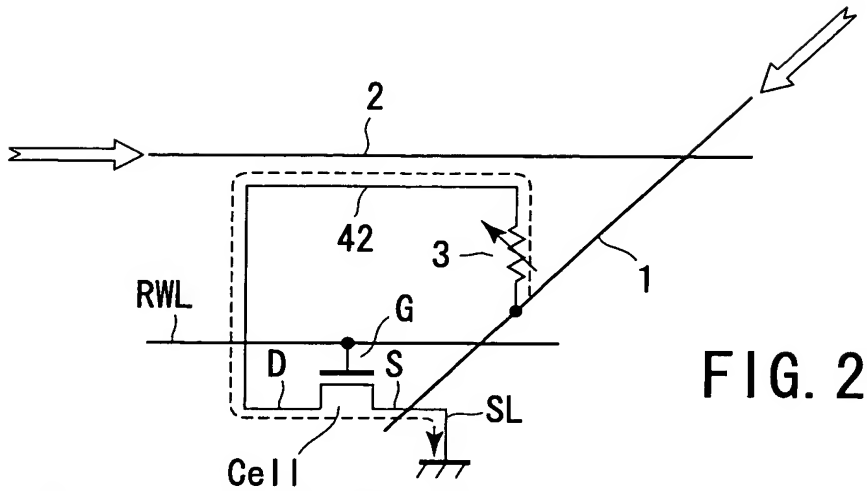

FIG. 24

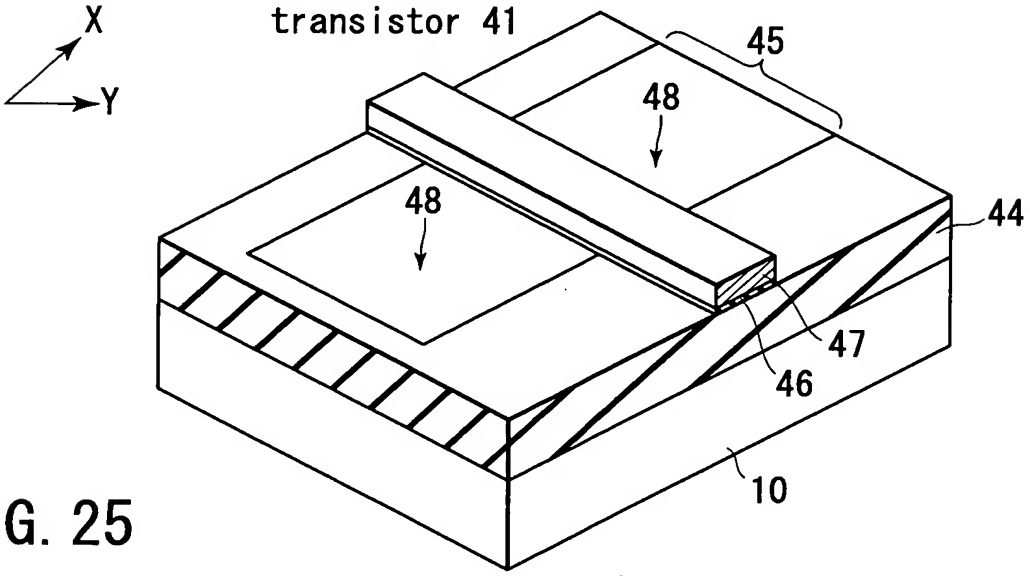

FIG. 25

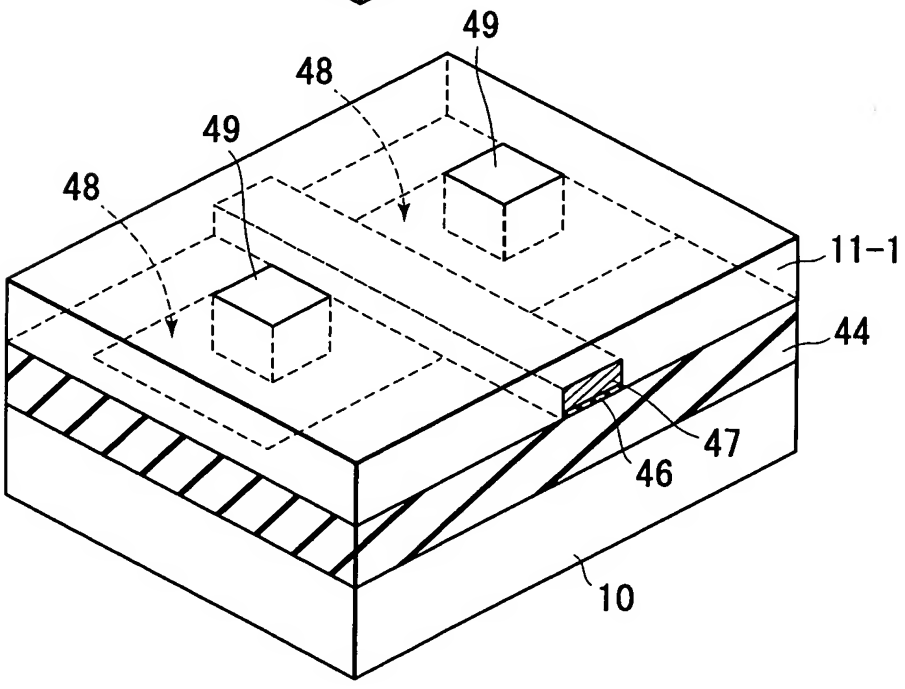

FIG. 26

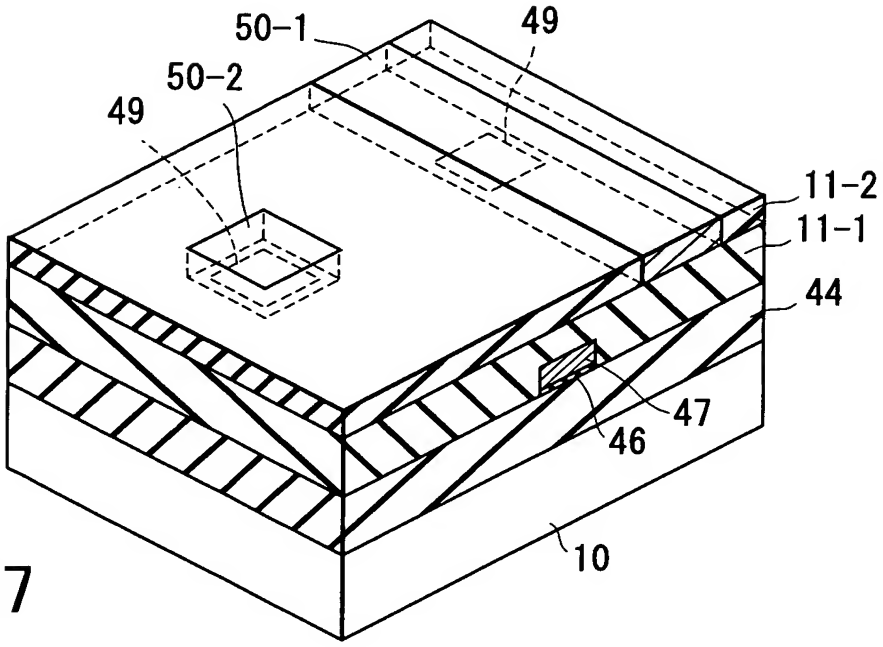
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FIG. 27

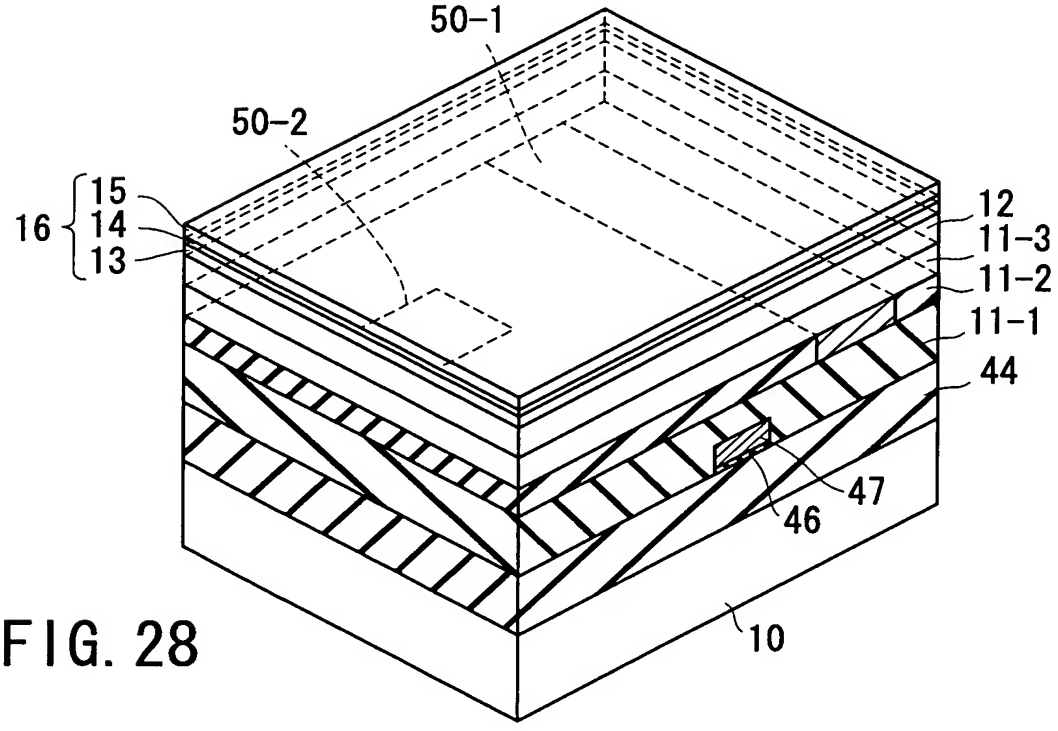
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FIG. 28

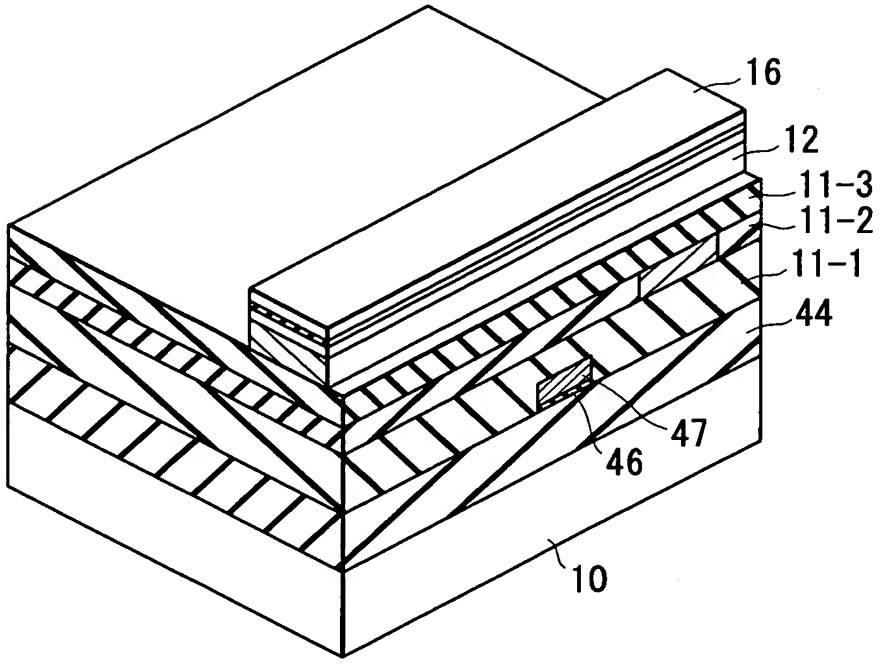

FIG. 29

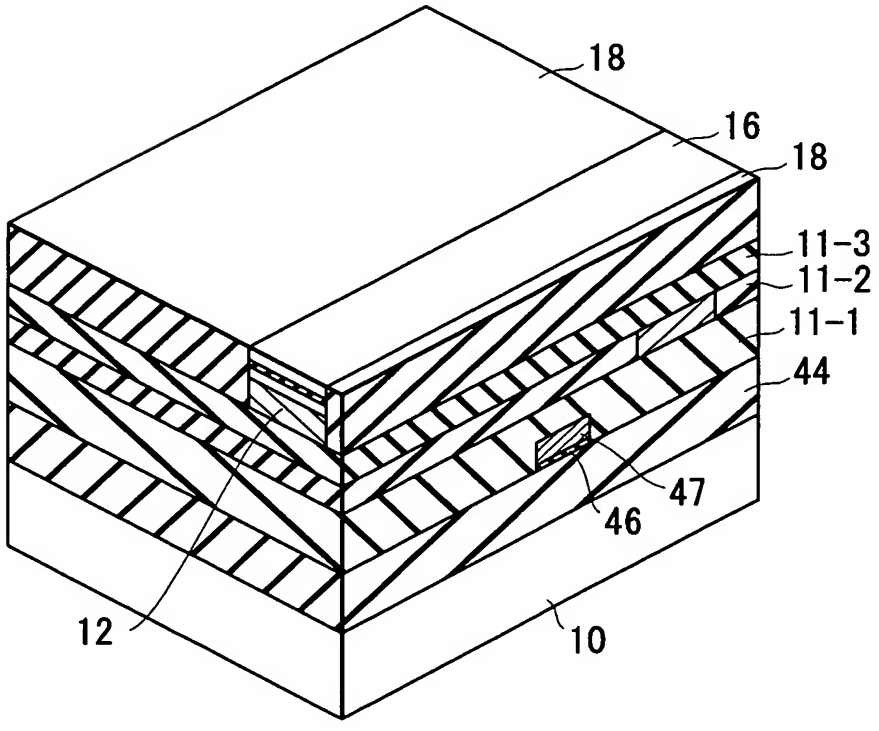

FIG. 30

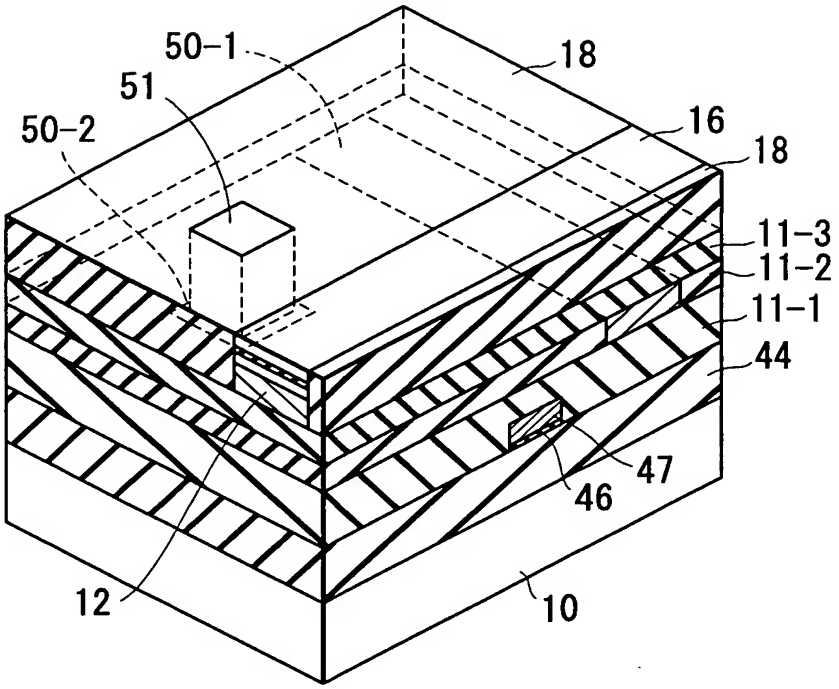
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FIG. 31

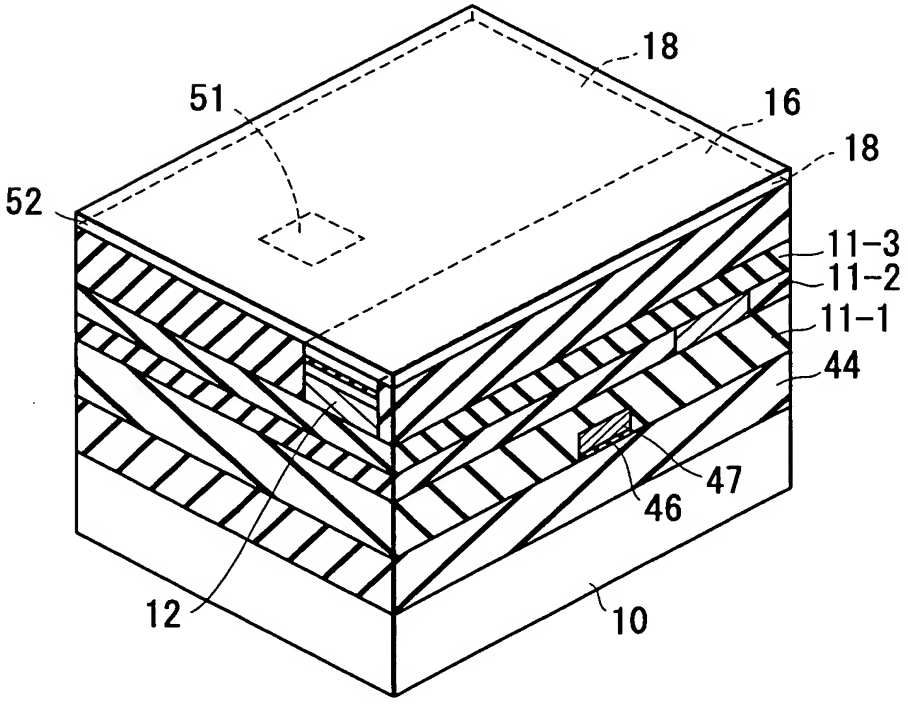
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FIG. 32

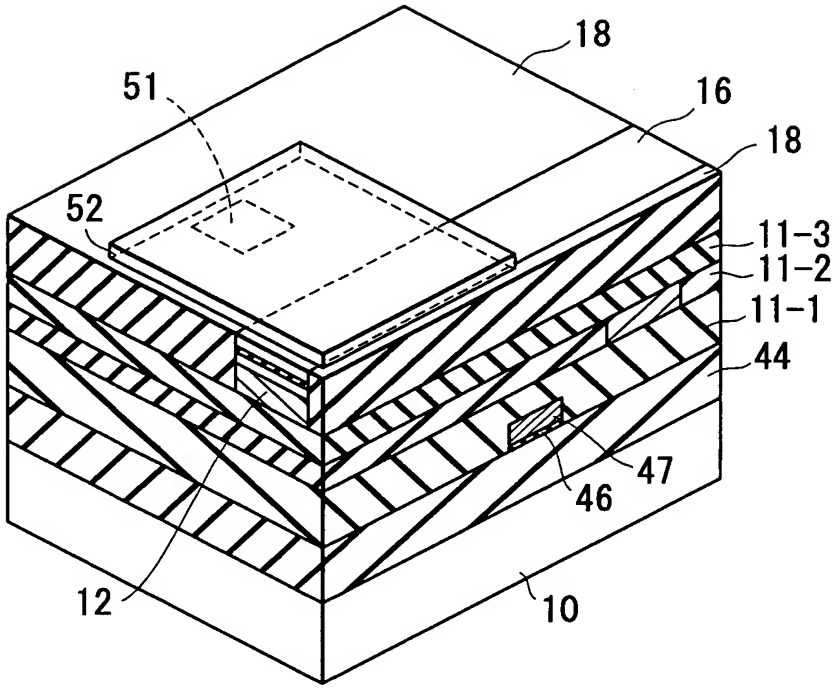
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FIG. 33

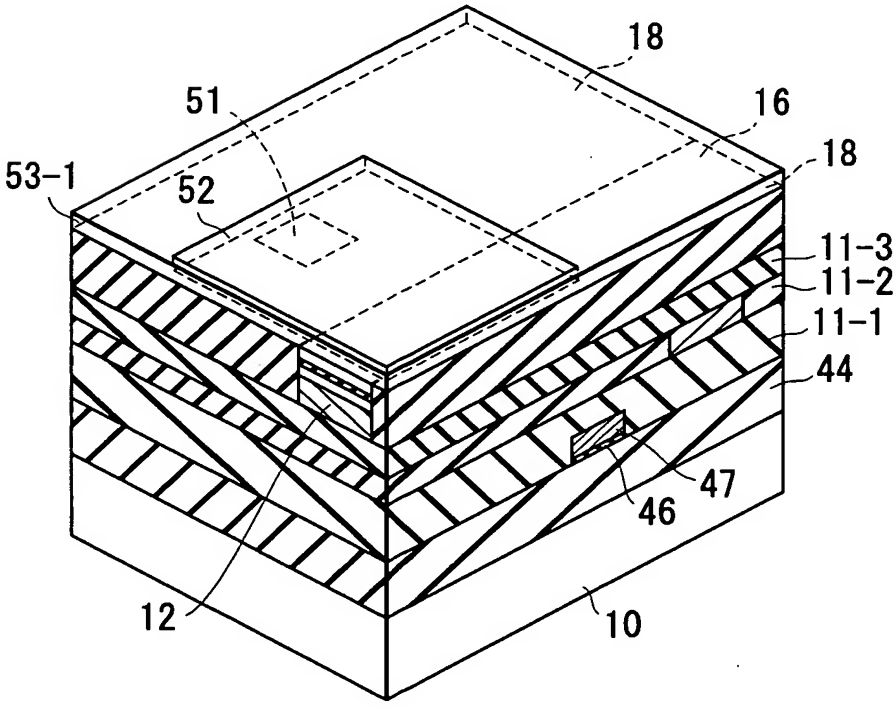
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FIG. 34

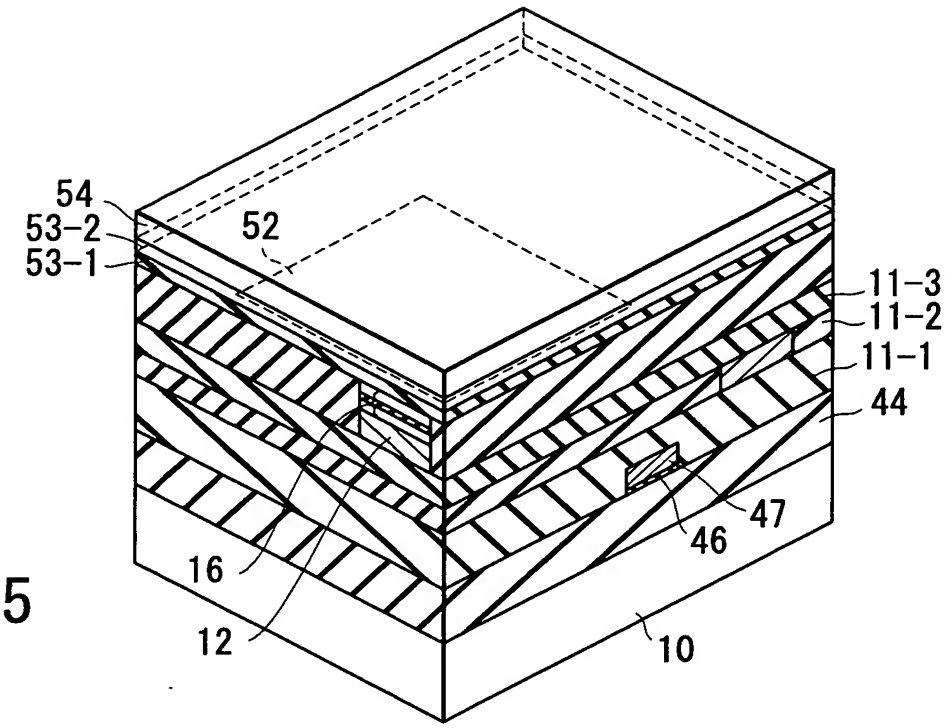
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FIG. 35

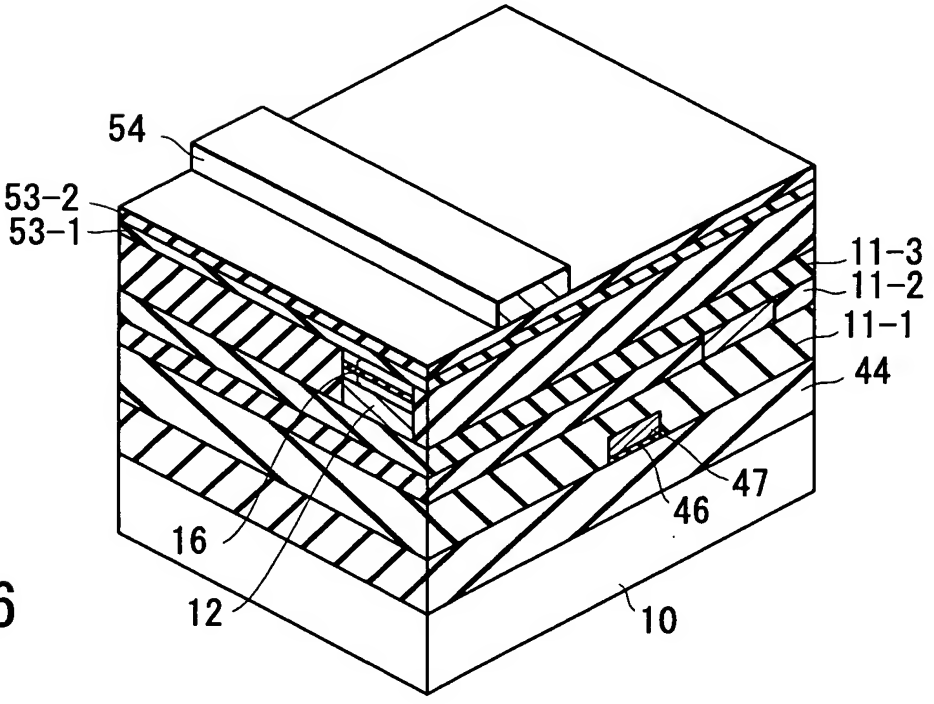
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FIG. 36

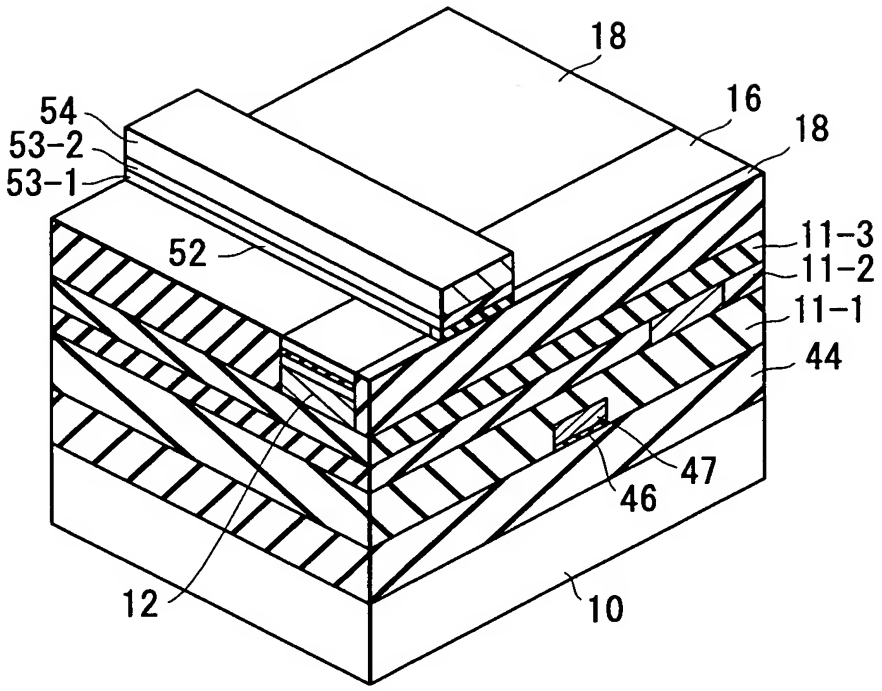
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FIG. 37

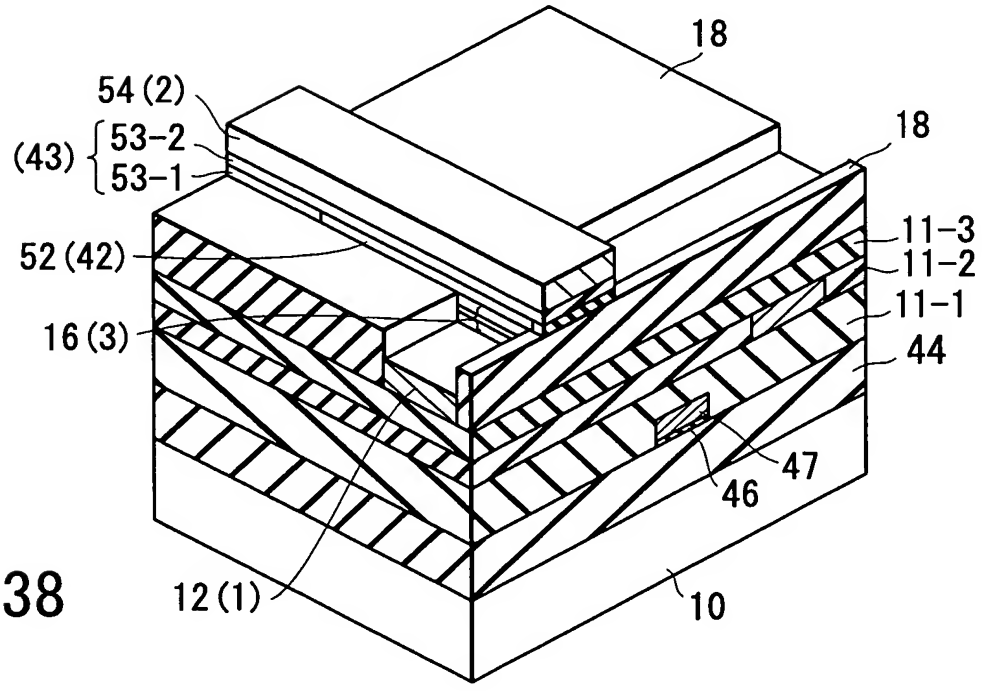
18
54 (2)
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FIG. 38

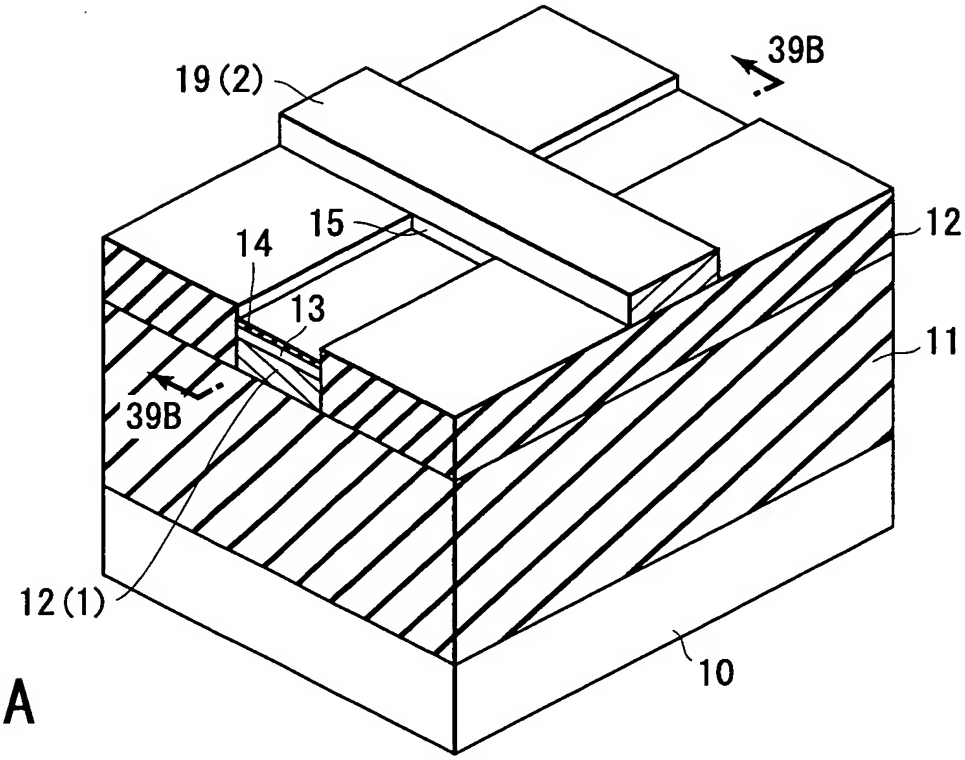

FIG. 39A

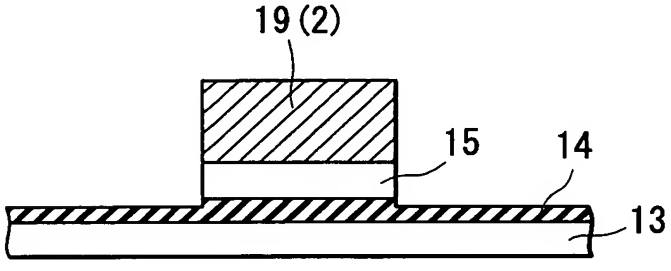

FIG. 39B

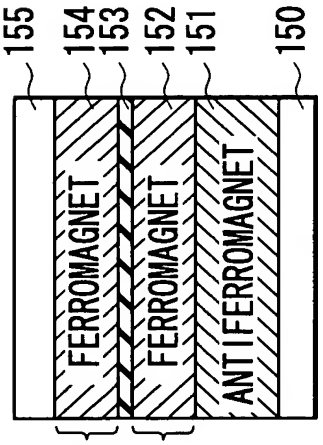

FIG. 40A

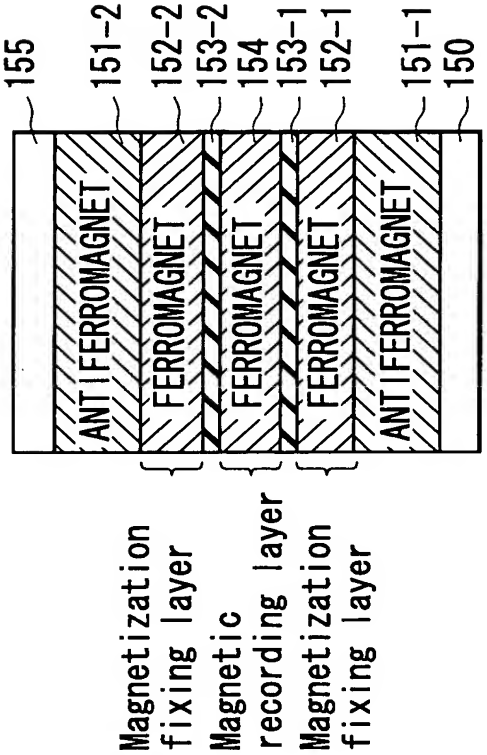

FIG. 40B

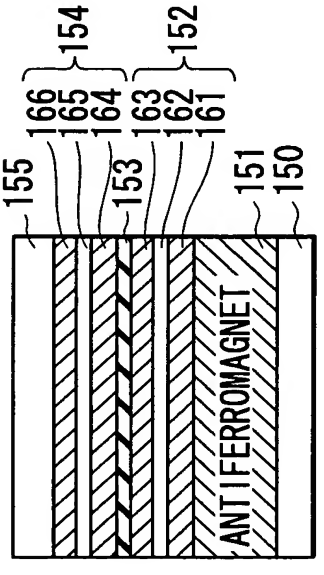

FIG. 40C

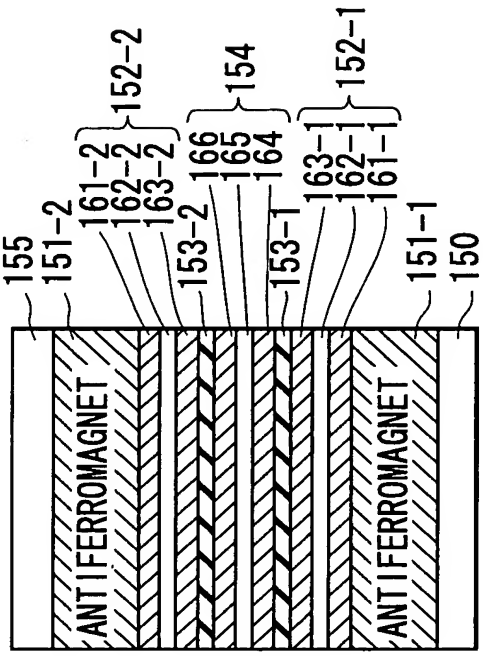

FIG. 40D

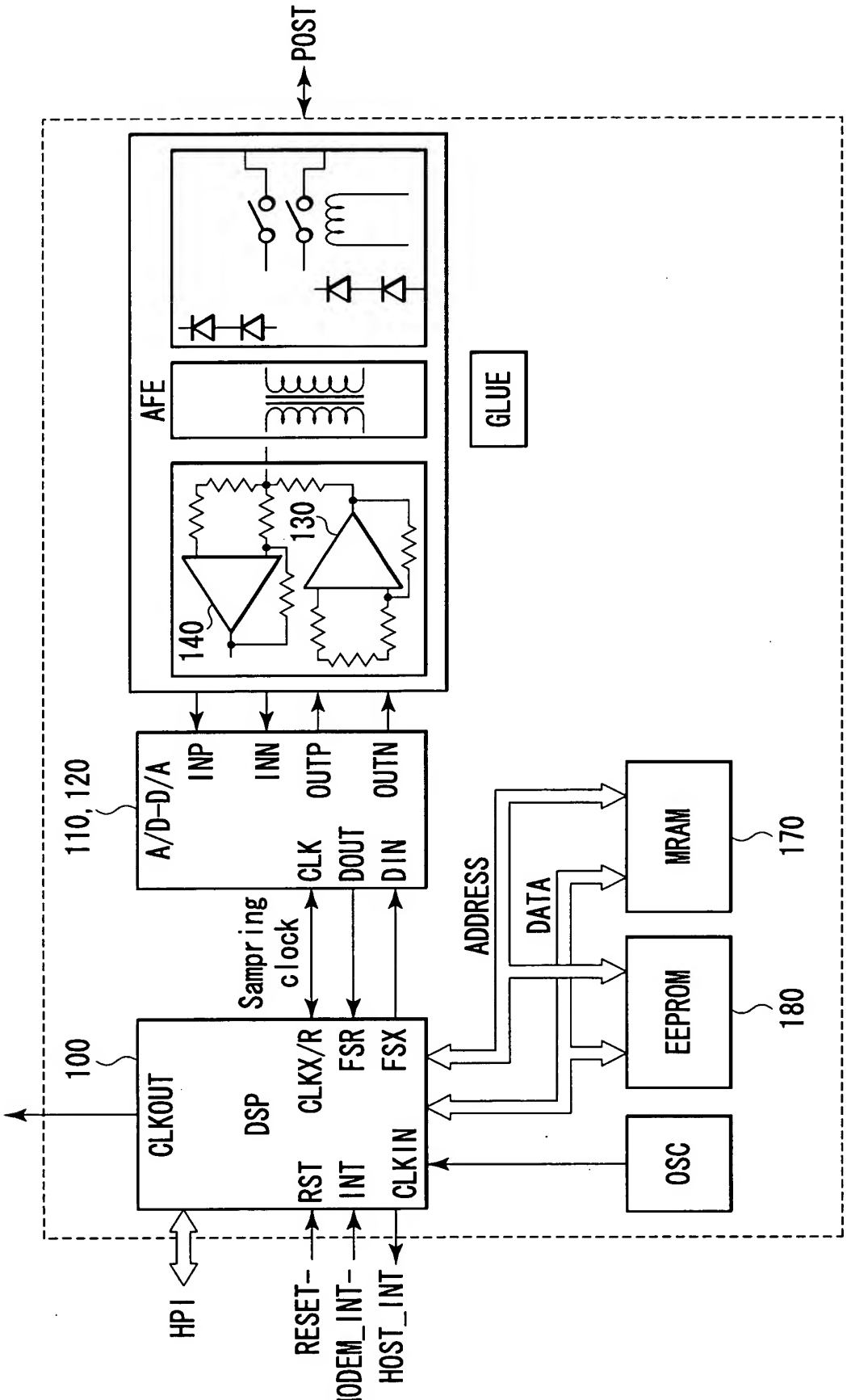
POST
AFE
GLUE
130
140
110, 120
A/D-D/A
INP
INN
OUTP
OUTN
CLK
DOUT
DIN
Sampring clock
ADDRESS
DATA
MRAM
170
EEPROM
180
OSC
100
CLKOUT
DSP
CLKX/R
FSR
FSX
RST
INT
CLKIN
HPI
RESET-
MODEM_INT-
HOST_INT

FIG. 41

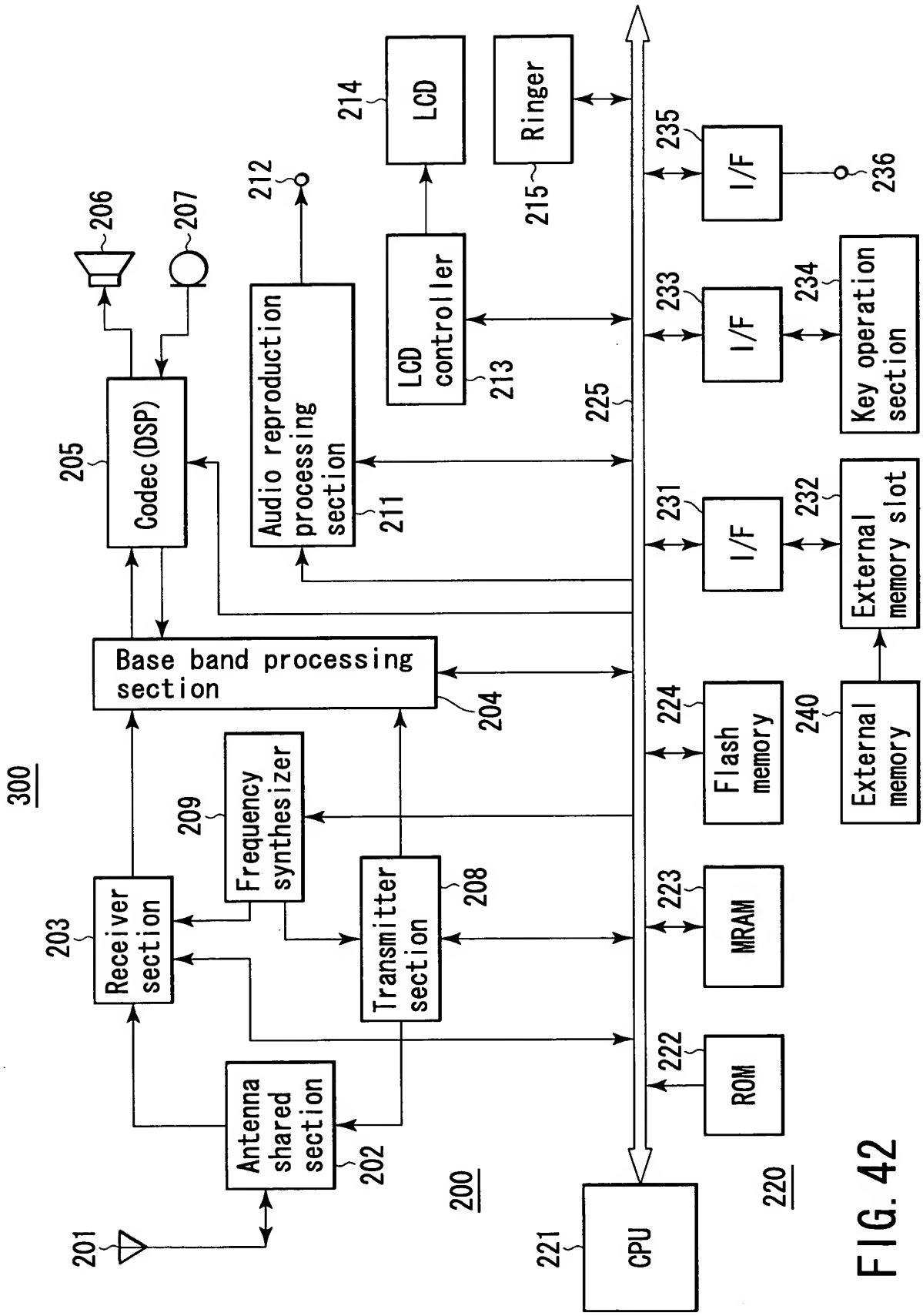
300
200
220
201
Antenna shared section
202
Receiver section
203
Transmitter section
208
Frequency synthesizer
209
Base band processing section
204
Codec (DSP)
205
206
207
Audio reproduction processing section
211
212
LCD controller
213
LCD
214
Ringer
215
225
I/F
231
External memory slot
232
I/F
233
Key operation section
234
I/F
235
236
Flash memory
224
External memory
240
MRAM
223
ROM
222
CPU
221

FIG. 42

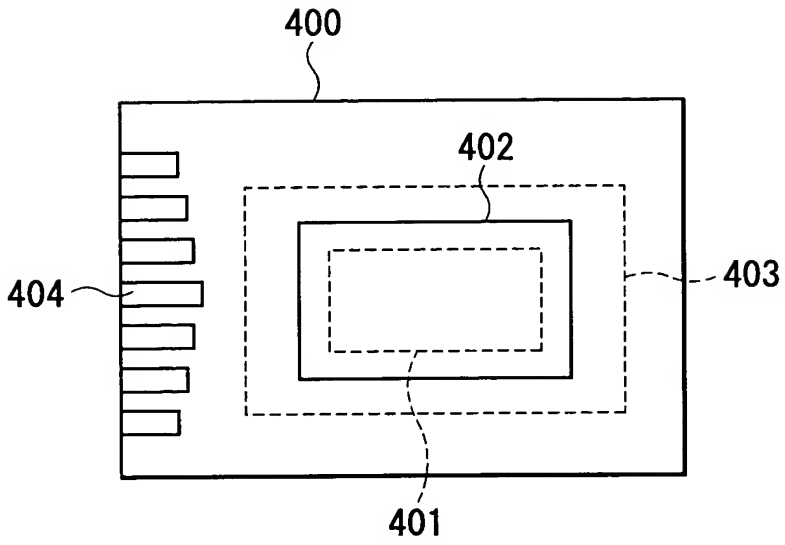
400
402
403
404
401

FIG. 43

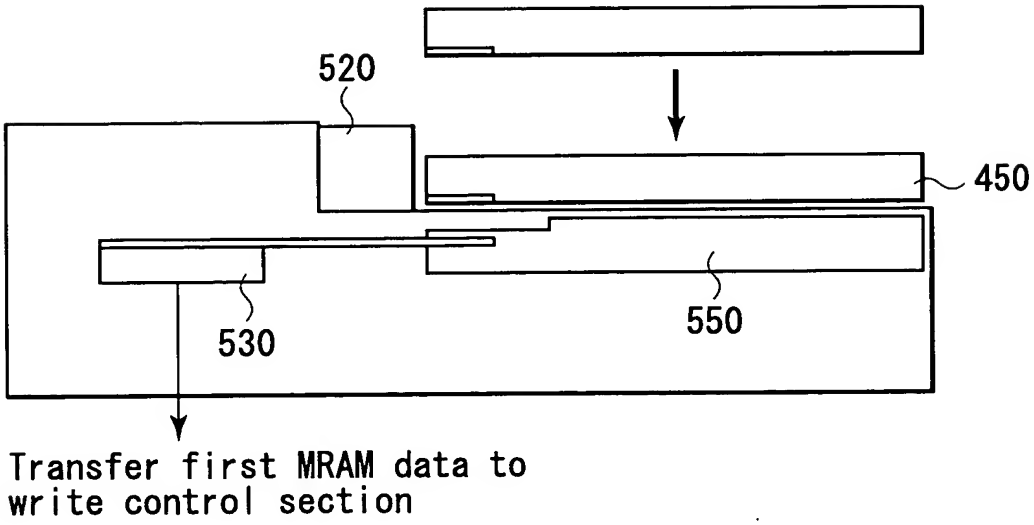
520
450
530
550
Transfer first MRAM data to
write control section

FIG. 46

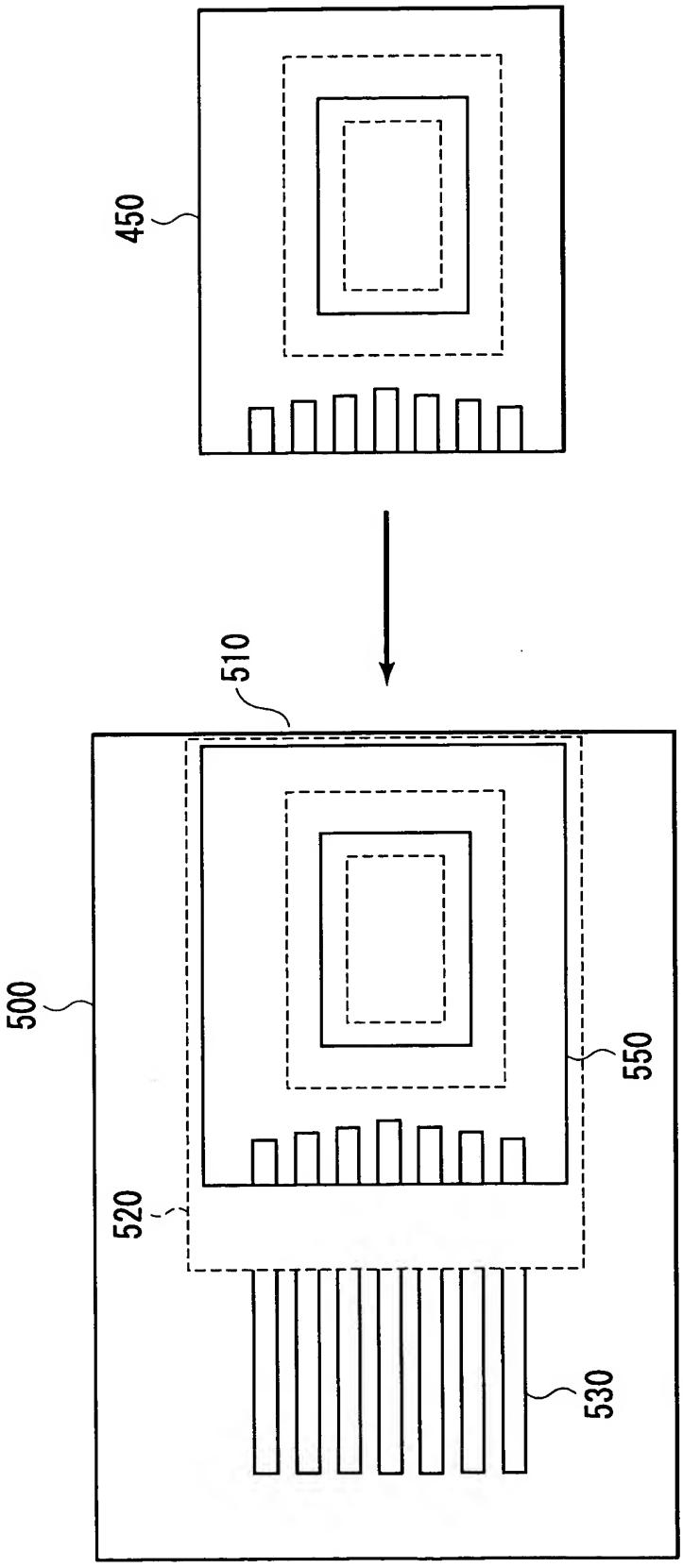

FIG. 44

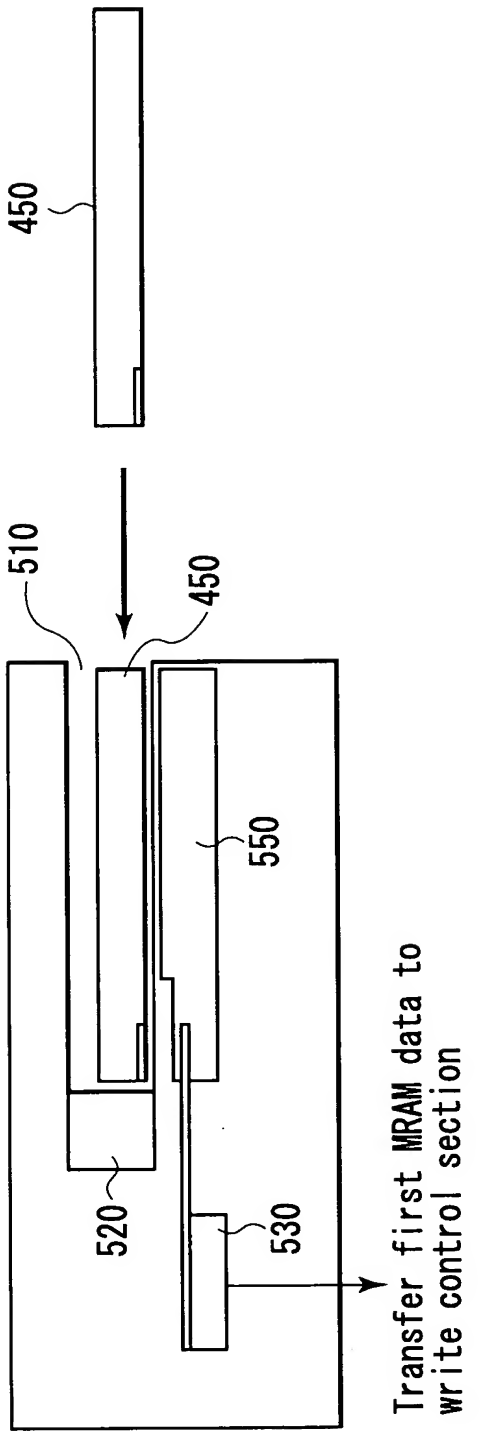
450
510
450
550
520
530
Transfer first MRAM data to write control section

FIG. 45

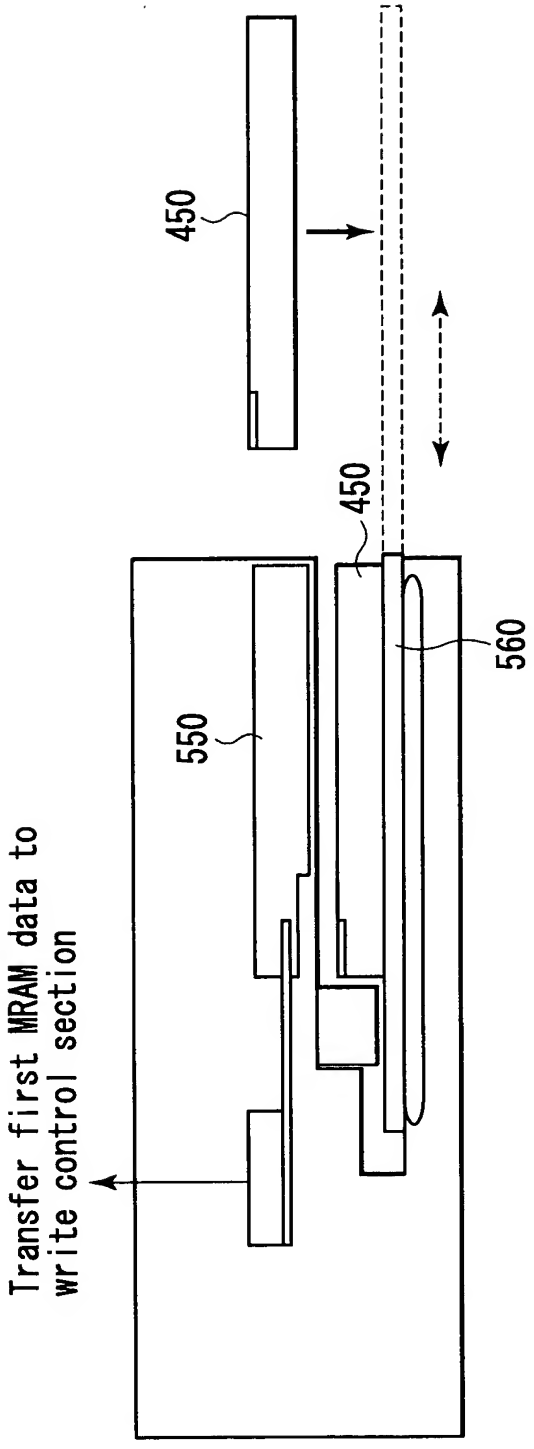
450
450
560
550
Transfer first MRAM data to write control section

FIG. 47

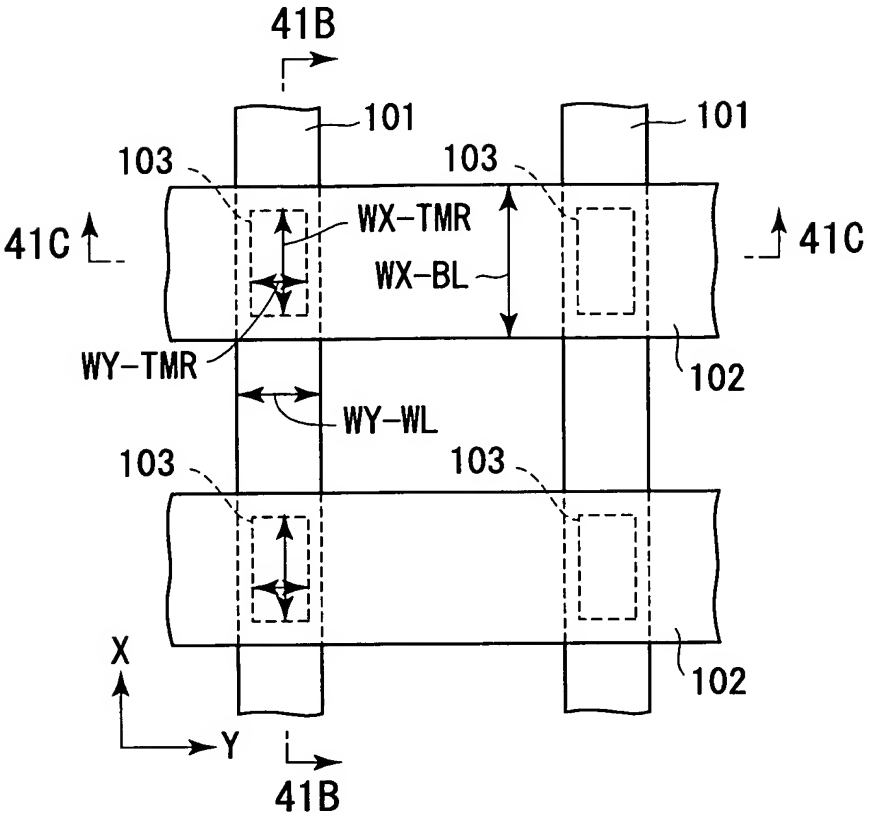

FIG. 48A

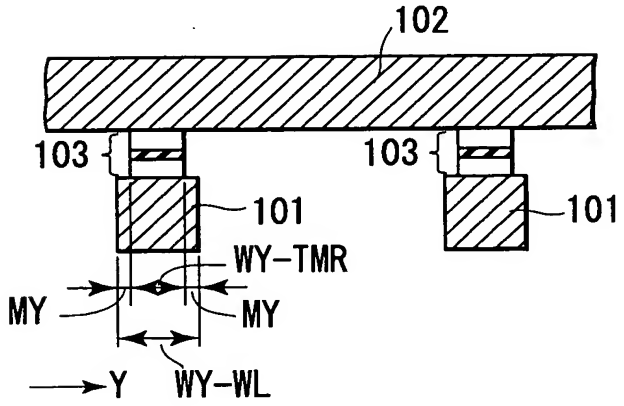

FIG. 48B

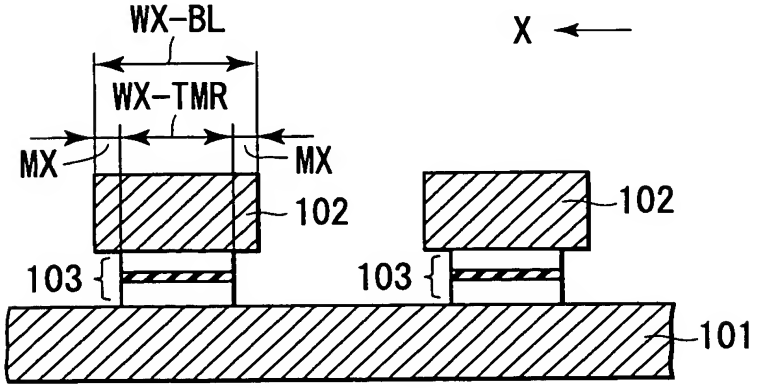

FIG. 48C

Ideal MTJ shape

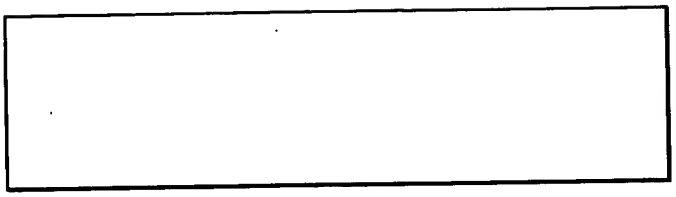

FIG. 49A

Ideal MTJ shape

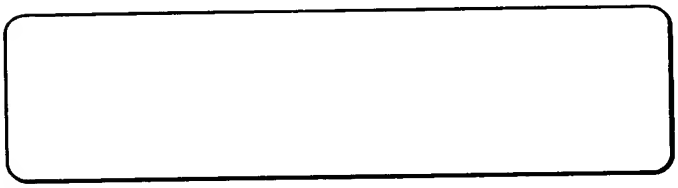

FIG. 49B

Actual MTJ shape

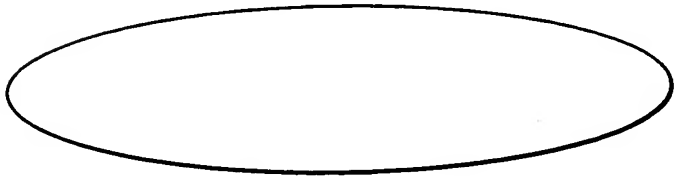

FIG. 49C